

# EE4109: Agenda (lecture 8)

1. Brief interactive lecture: Design of output stages
2. Instructions: Design of output stage
  1. Requirements drive capability
  2. Type of stage
  3. Design considerations for W, L and Biasing
  4. Minimum geometry of device(s)
3. Homework: SLiCAP output stage, see BrightSpace



order of designing		independent performance aspects									
1	2	3	4	5	6	7	8	9			
type	gain	noise	power efficiency	clipping	small-signal bandwidth	frequency response	weak nonlinearity	DC (temperature) stability			
feedback configuration	☺	☺	☺	☺	☺	☺	☺	☺	X		
feedback network	☺	☺	☺	☺	☺	☺	☺	☺	X		
controller input stage	☺	☺	☺	☺	☺	☺	☺	☺	X		
controller output stage type	☺	☺	☺	☺	☺	☺	☺	☺	X		
controller output stage biasing	☺	☺	☺	☺	☺	☺	☺	☺	X		
loop gain poles product	☺	☺	☺	☺	☺	☺	☺	☺	X		
frequency compensation	☺	☺	☺	☺	☺	☺	☺	☺	X		
differential error to gain ratio	☺	☺	☺	☺	☺	☺	☺	☺	X		
over-all biasing	☺	☺	☺	☺	☺	☺	☺	☺	X		

Orthogonal design