EE4109: Agenda (lecture 8)

1. Discussion homework
   - What do we learn here?
   - Critical use of tools and models
2. Instructions: Design of output stage
   1. Requirements drive capability
   2. Type of stage
   3. Design considerations for W, L and Biasing
   4. Minimum geometry of device(s)
3. Homework: SLiCAP output stage, see BrightSpace