

# EE4109: Agenda (lecture 8)

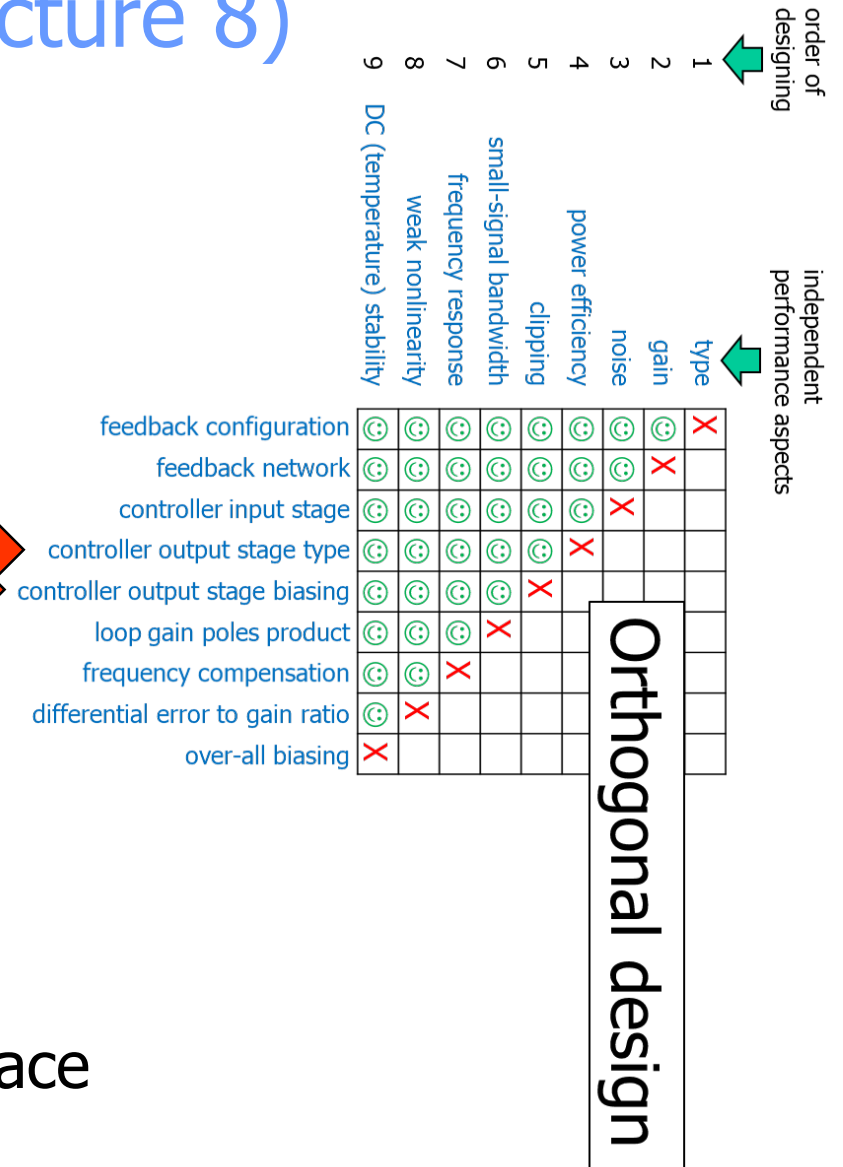
## 1. Discussion homework

- What do we learn here?
- Critical use of tools and models

## 2. Instructions: Design of output stage

1. Requirements drive capability
2. Type of stage
3. Design considerations for W, L and Biasing
4. Minimum geometry of device(s)

## 3. Homework: SLiCAP output stage, see BrightSpace



The table illustrates an orthogonal design for the output stage design. It maps 10 independent performance aspects (rows) against 9 different design orders (columns). Each cell contains a smiley face (:) indicating a valid design point or a red 'X' indicating a conflict. Two large red arrows point from the 'Design of output stage' section to the 'controller output stage type' and 'controller output stage biasing' rows.

independent performance aspects	1	2	3	4	5	6	7	8	9
type	X	:	:	:	:	:	:	:	:
gain	:	X	:	:	:	:	:	:	:
noise	:	:	X	:	:	:	:	:	:
power efficiency	:	:	:	X	:	:	:	:	:
clipping	:	:	:	:	X	:	:	:	:
small-signal bandwidth	:	:	:	:	:	X	:	:	:
frequency response	:	:	:	:	:	:	X	:	:
weak nonlinearity	:	:	:	:	:	:	:	X	:
DC (temperature) stability	:	:	:	:	:	:	:	:	X

Orthogonal design