

Structured Electronic Design

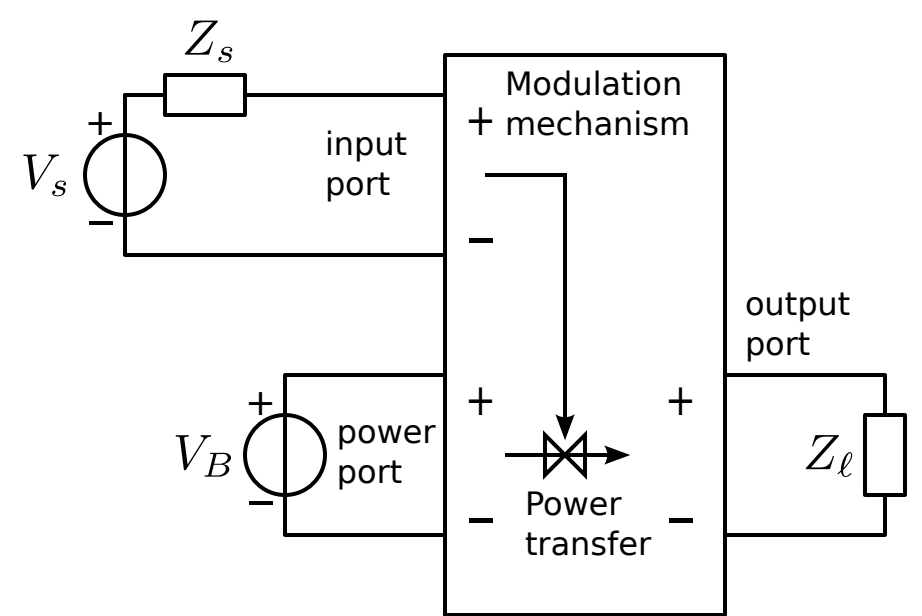
EE4109

Course program

Anton J.M. Montagne

Principle of amplification and biasing

Modulation of power transfer from power source to the load by the signal source



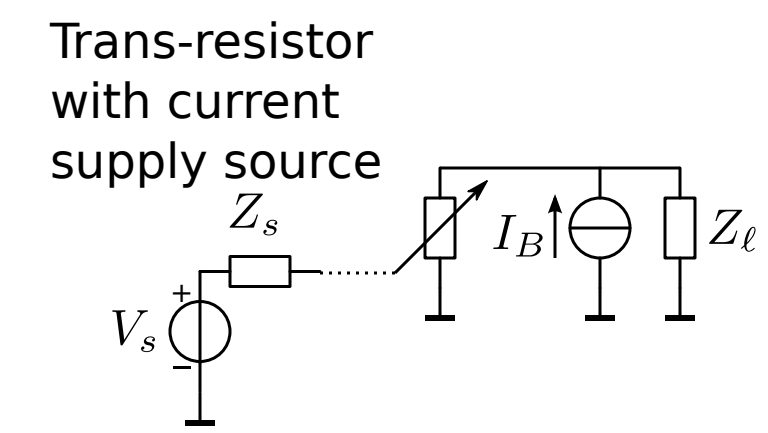
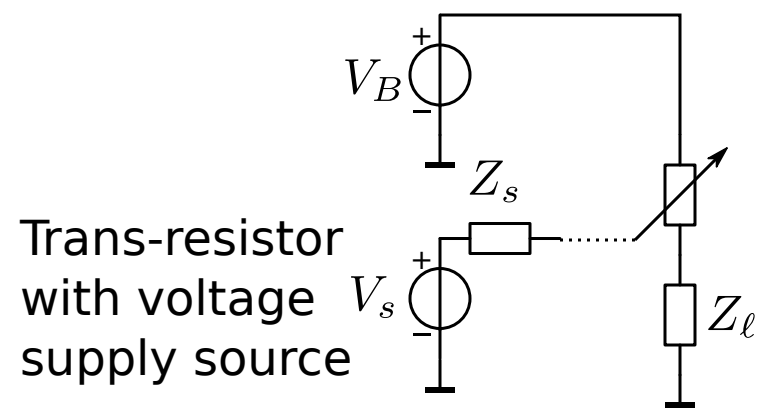
Modulation of a current through a passive device:

A. Search for a device:

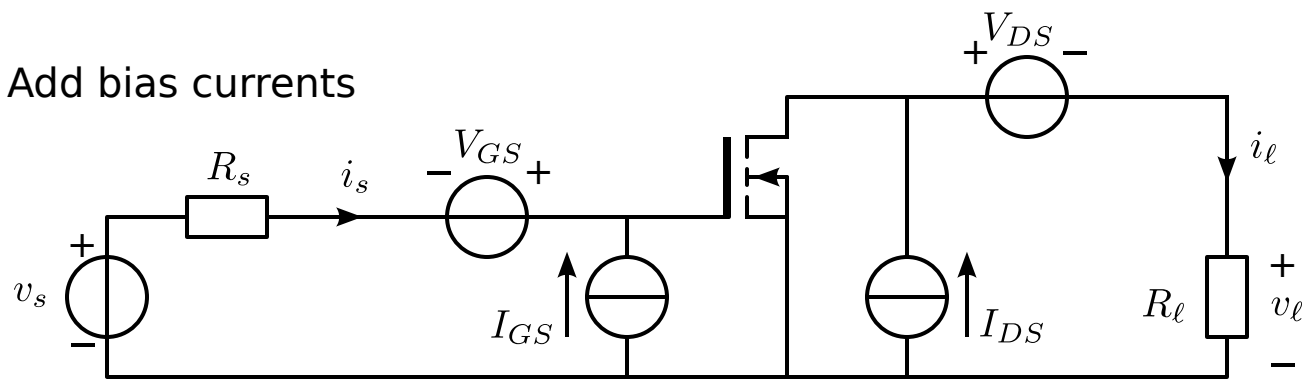
- 1. Two-terminal device with nonlinear v-i characteristic
- 2. Two-port device with output v-i characteristic controlled by its input voltage or current

C. Create a current through this device

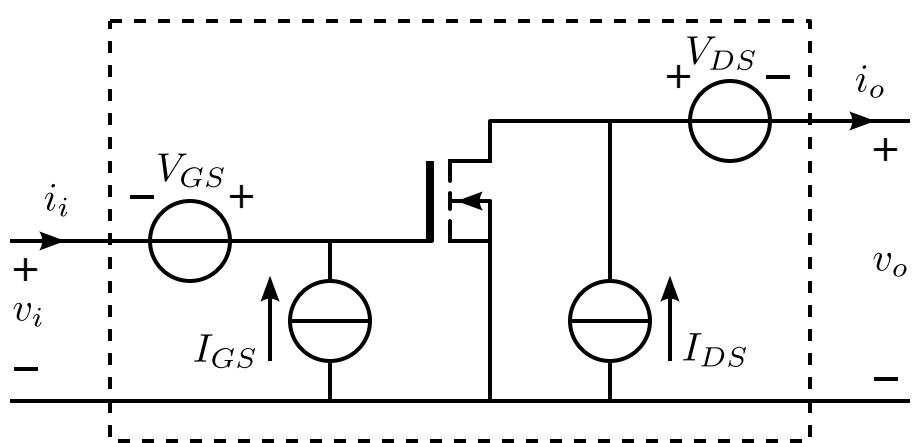
- 1. Apply a bias source at the output



Add bias currents

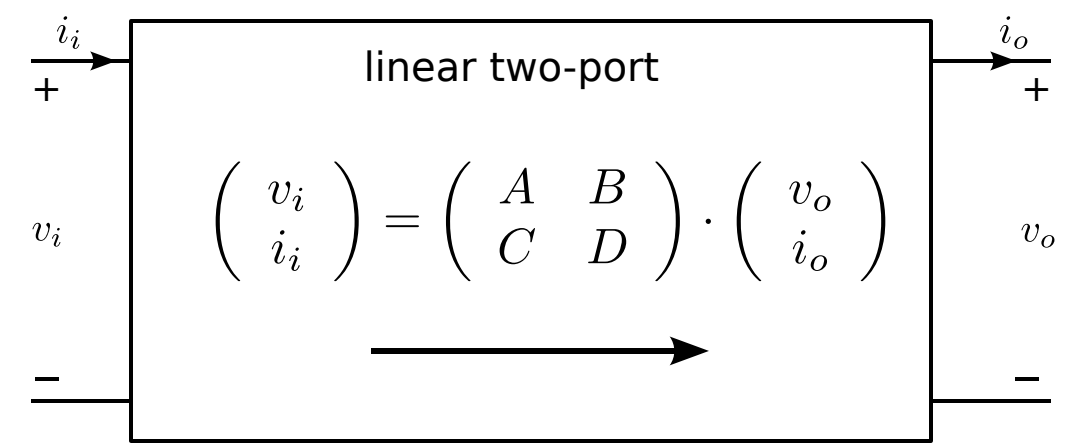


No bias currents flow through the source and the load
 $(v_s, v_\ell), (v_s, i_\ell), (i_s, v_\ell), (i_s, i_\ell)$ characteristics pass through the origin



Biased amplifier stage
Bias power delivered by I_{GS} and I_{DS}

Linearization in the operating point:

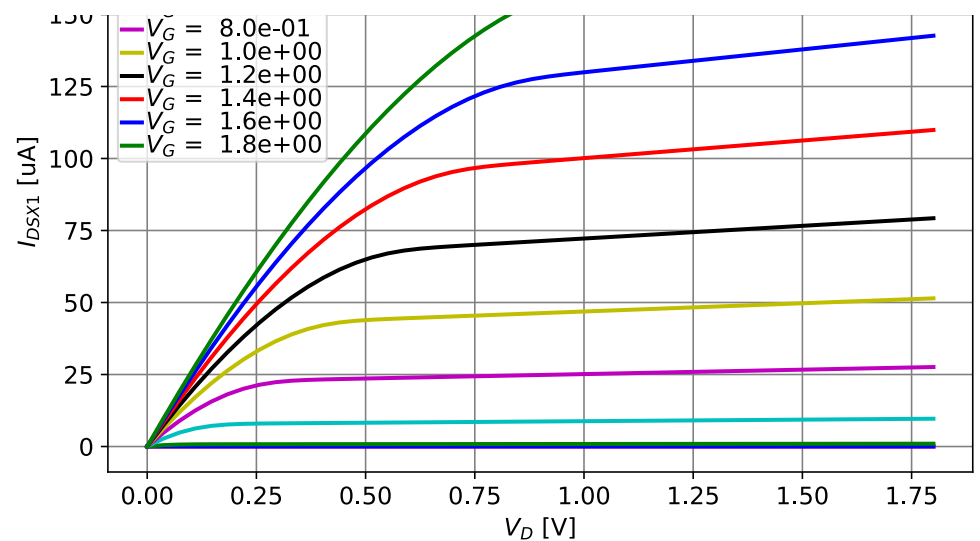
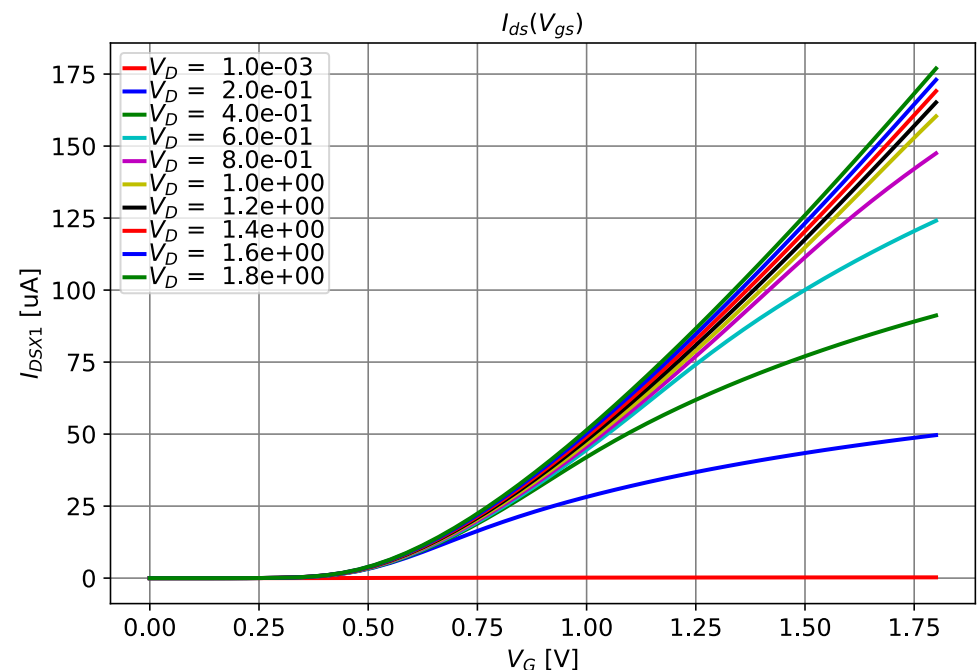
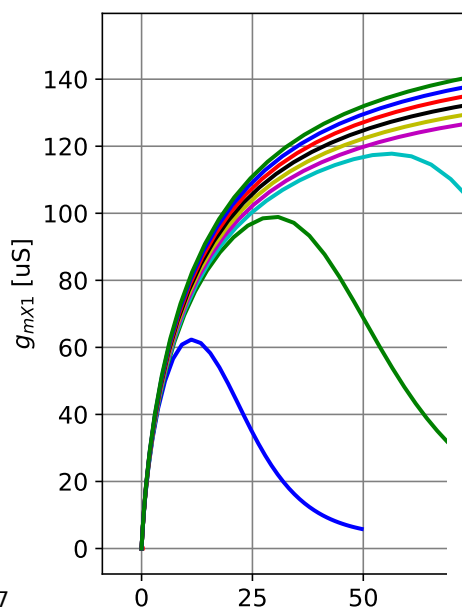
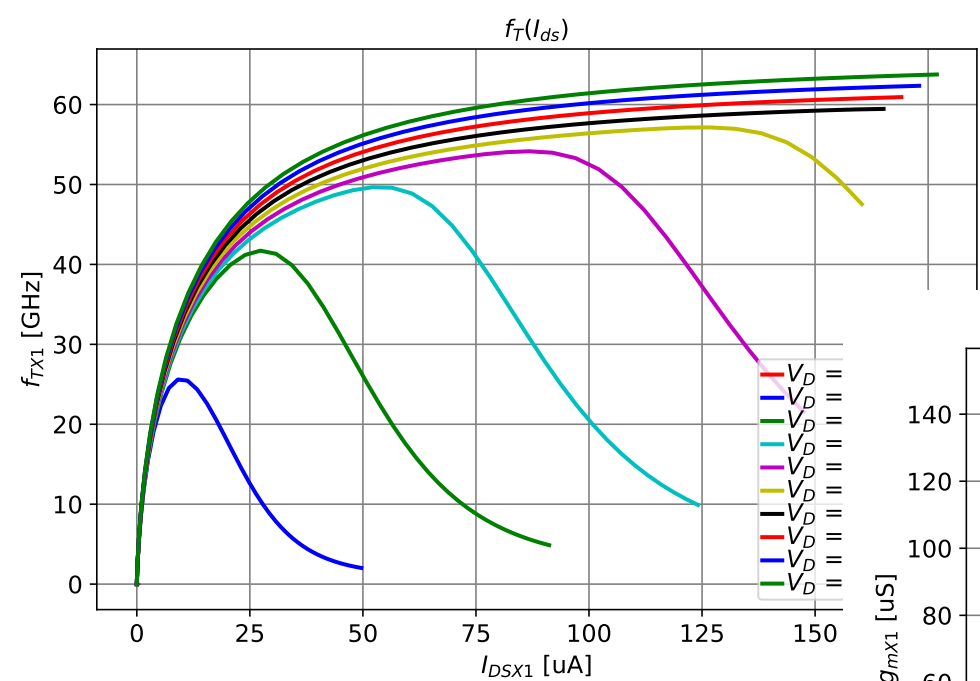


Maximum available power gain of a unilateral linear resistive two-port:

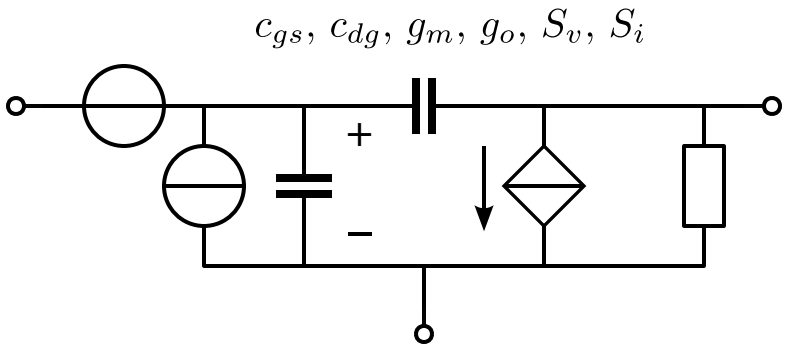
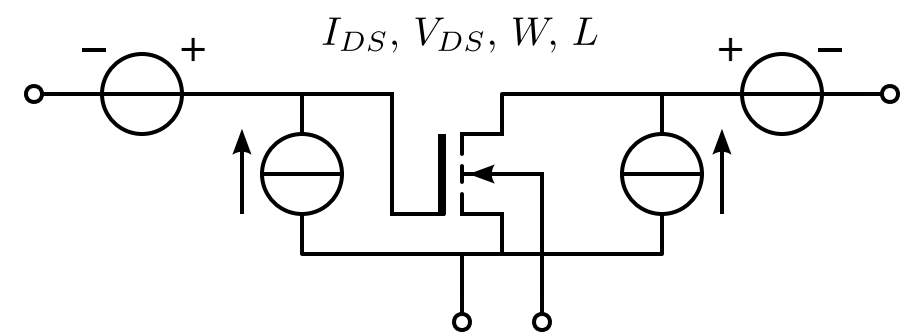
$$P_{av,max} = \frac{1}{4AD}$$

Amplifying devices

Estimate amplifying capabilities and limitations
from device characteristics, geometry and operating conditions



```
.model C18nmos nmos (  
+level=49  
+noimod=1 version=3.1 tnomo=27 tox=4.1E-9 xj=1E-7 nch=2.3549E17 vth0=0.362587  
+k1=0.5865832 k2=4.152205E-3 k3=1E-3 k3b=2.1824687 w0=1E-7 nlx=1.795622E-7  
+dvt0w=0 dvt1w=0 dvt2w=0 dvt0=1.746117 dvt1=0.4409233 dvt2=-3.663487E-4  
+u0=262.117234 ua=-1.386325E-9 ub=2.284255E-18 uc=5.506514E-11 vsat=1.04174E5 a0=1.9287698  
+ags=0.416466 b0=-1.536637E-9 b1=-1E-7 keta=-7.111387E-3 a1=6.573435E-4 a2=0.8808358  
+rds=112.5093924 prwg=0.494777 prwb=-0.2 wr=1 wint=7.098292E-9 lint=1.120392E-8  
+xl=-2E-8 xw=-1E-8 dwg=-3.812756E-9 dwb=8.690068E-9 voff=-0.0878502 nfactor=2.2975194  
+cit=0 cdsc=2.4E-4 cdscd=0 cdsb=0 eta0=3.116078E-3 etab=1  
+dsb=0.0226021 pclm=0.7222753 pdiblc1=0.2160258 pdiblc2=2.237807E-3 pdiblc3=0.1 drout=0.8036712  
+pscbe1=5.434136E8 pscbe2=1e-3 pvag=1e-12 delta=0.01 rsh=6.8 mobmod=1 prt=0 ute=-1.5  
+kt1=-0.11 kt1l=0 kt2=0.022 ua1=4.31E-9 ub1=-7.61E-18 uc1=-5.6E-11 at=3.3E4 wl=0 wln=1 ww=0  
+wwn=1 ww=0 ll=0 ll=1 lw=0 lwn=1 lwl=0 capmod=2 xpart=0.5  
+cgdo=6.99E-10 cgso=6.99E-10 cgbo=1E-12 cj=9.840057E-4 pb=0.7342005 mj=0.3623465  
+cjs=2.405513E-10 pbsw=0.4681508 mjs=0.1 cjs=3.3E-10 pbsw=0.4681508 mjs=0.1  
+cf=0 pvth0=-7.11401E-4 prdsw=-0.6661763 pk2=5.920718E-4 wketa=2.148339E-4 lketa=-0.0151118  
+pu0=3.3563216 pua=-1.30682E-11 pub=0 pvsat=1.25639E3 peta0=1E-4 pketa=6.507934E-4  
+kf=4.5E-29 )
```



EKV model

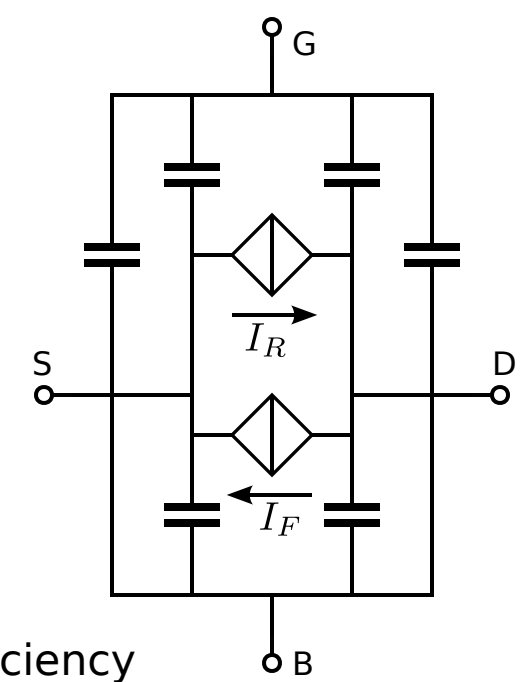
Cut-off frequency

Inversion coefficient

Transconductance efficiency

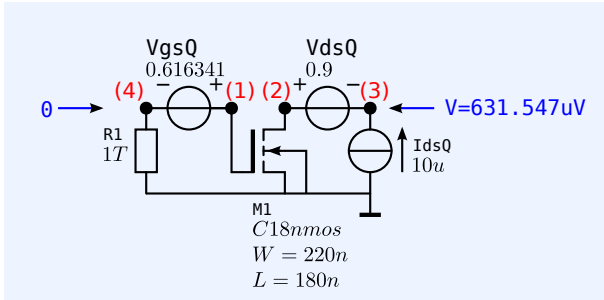
Critical inversion coefficient

1/f noise corner frequency

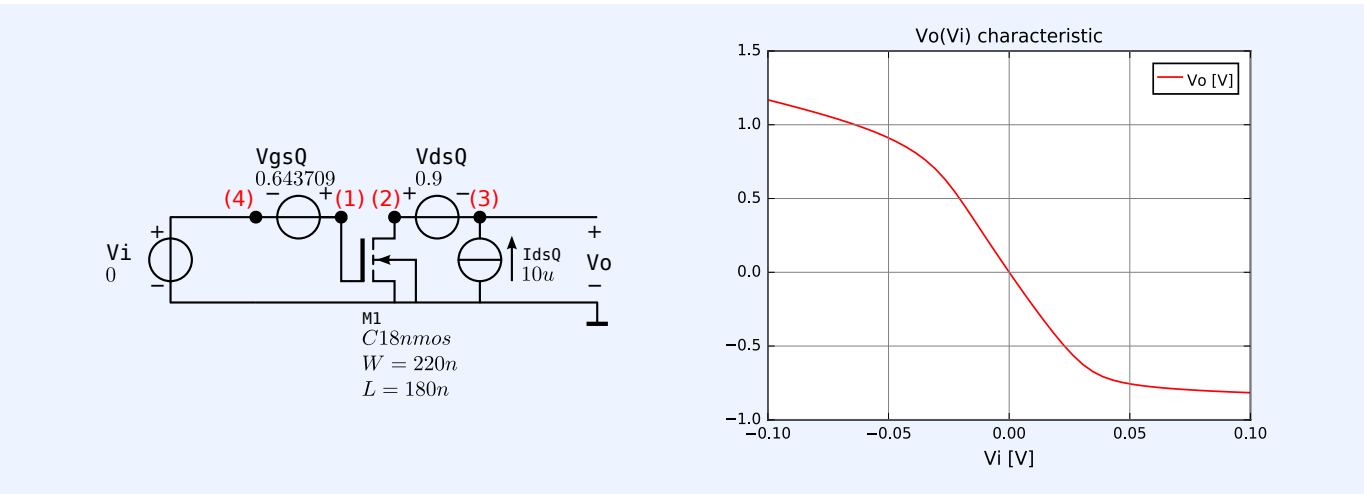


```
.subckt CMOS18N drain gate source bulk W={W} L={L} ID={ID}  
* EKV model of transistor without bulk resistances  
* Voltage dependency of bulk capacitances not modeled  
* Operating in forward saturation region  
*  
M1 drain gate source bulk CMOS18N  
  
.model CMOS18N M  
+ gm = {g_m}  
+ go = {g_o}  
+ gb = {g_b}  
+ cgs = {c_gs}  
+ cdg = {c_dg}  
+ cgb = {c_gb}  
+ cdb = {c_db}  
+ csb = {c_sb}  
* Parameters will be substituted if simType has been set to "numeric"  
.param  
* device equations EKV model  
* See Binkley: "Tradeoffs and Optimization in Analog CMOS Design"  
+ IC_CRIT = {1/(4*(N_s_N18*U_T)*(Theta_N18+1/L/E_CRIT_N18))^2}  
+ g_m = {ID/(N_s_N18*U_T*sqrt(IC*(1+IC/IC_CRIT)+0.5*sqrt(IC*(1+IC/IC_CRIT))+1))}  
+ g_o = {ID/VAL_N18/L}  
+ g_b = {(N_s_N18-1)*g_m}  
+ c_gs = {2/3*W*L*C_OX_N18 + CGSO_N18*W}  
+ c_dg = {CGSO_N18*W}  
+ c_gb = {CGBO_N18*2*L+(N_s_N18-1)/N_s_N18*C_OX_N18*W*L/3}  
+ c_db = {CJB0_N18*W*LDS_N18}  
+ c_sb = {CJB0_N18*W*LDS_N18}  
+ IC = {ID*L/W/I_0_N18}  
+ V_GS = {2*N_s_N18*U_T*ln(exp(sqrt(IC))-1)+Vth_N18}  
+ f_T = {g_m/2/pi/c_iss}  
+ c_iss = {c_gs+c_dg+c_gb}  
.ends
```

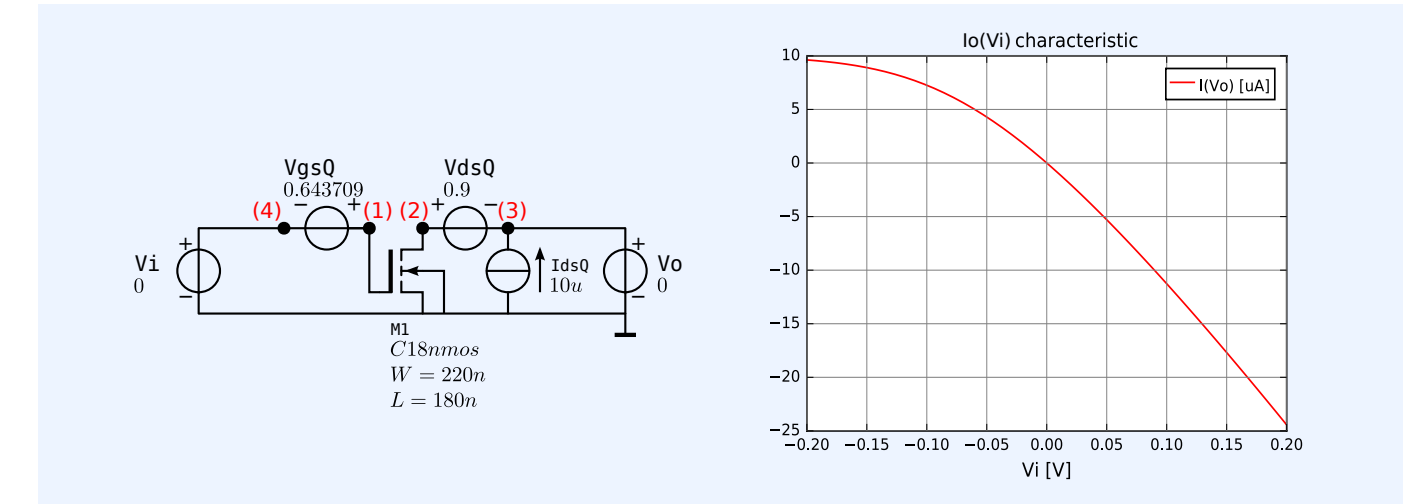
CS stage static and dynamic behavior



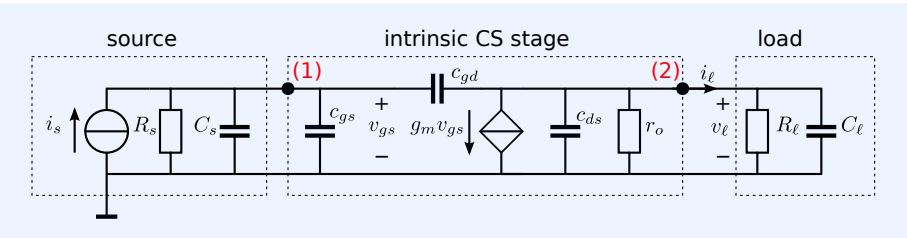
biased stage



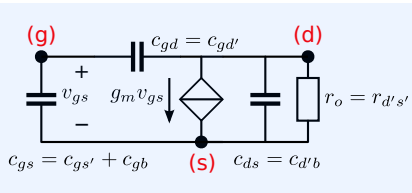
static voltage drive capability



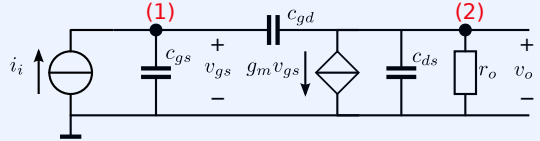
static current drive capability



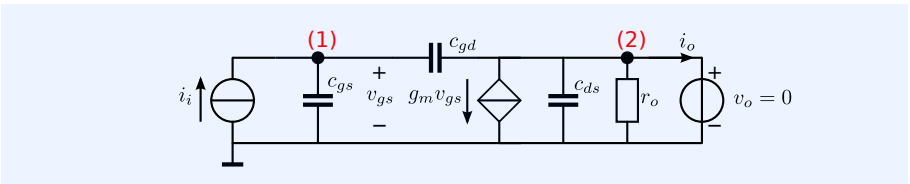
small-signal source-to-load transfer



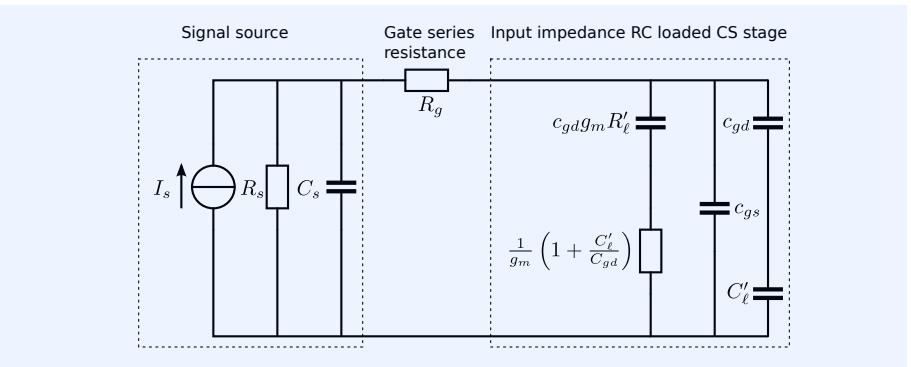
small-signal model



small-signal transimpedance



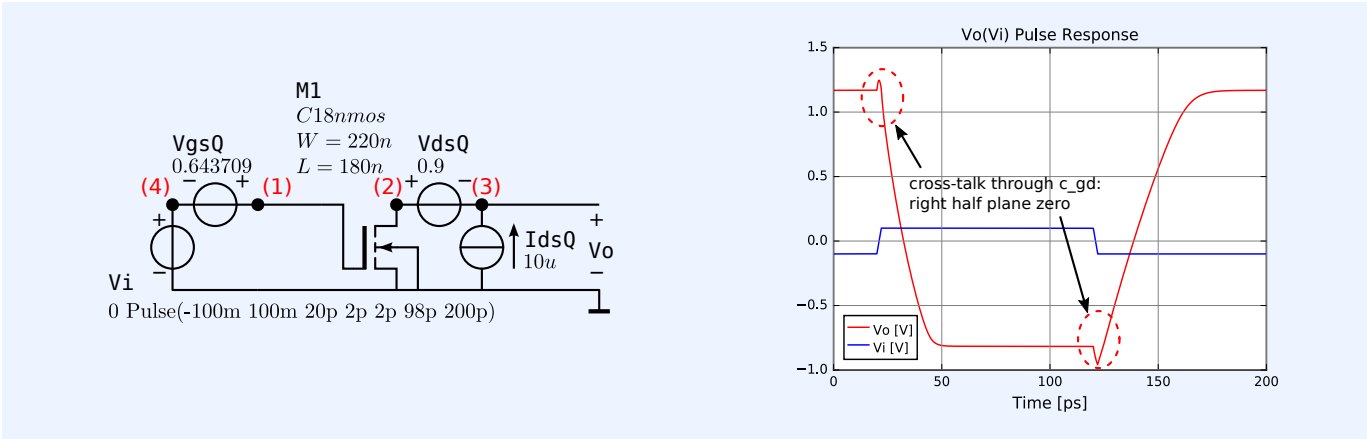
small-signal current gain



small-signal voltage driven

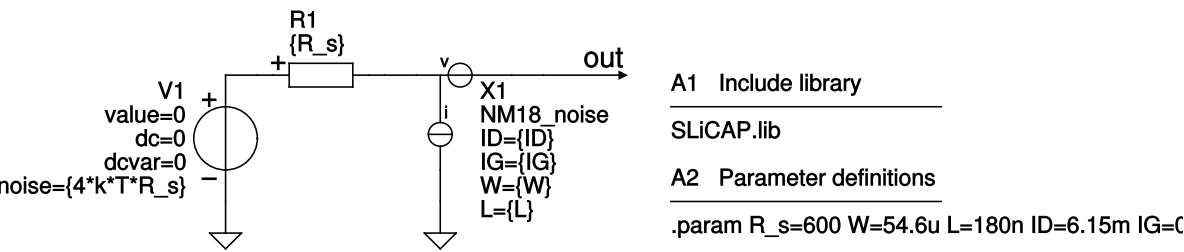
Study behavior

Find design parameters for performance aspects



dynamic voltage drive capability

Circuit Data



Netlist: CS stage resistive noise

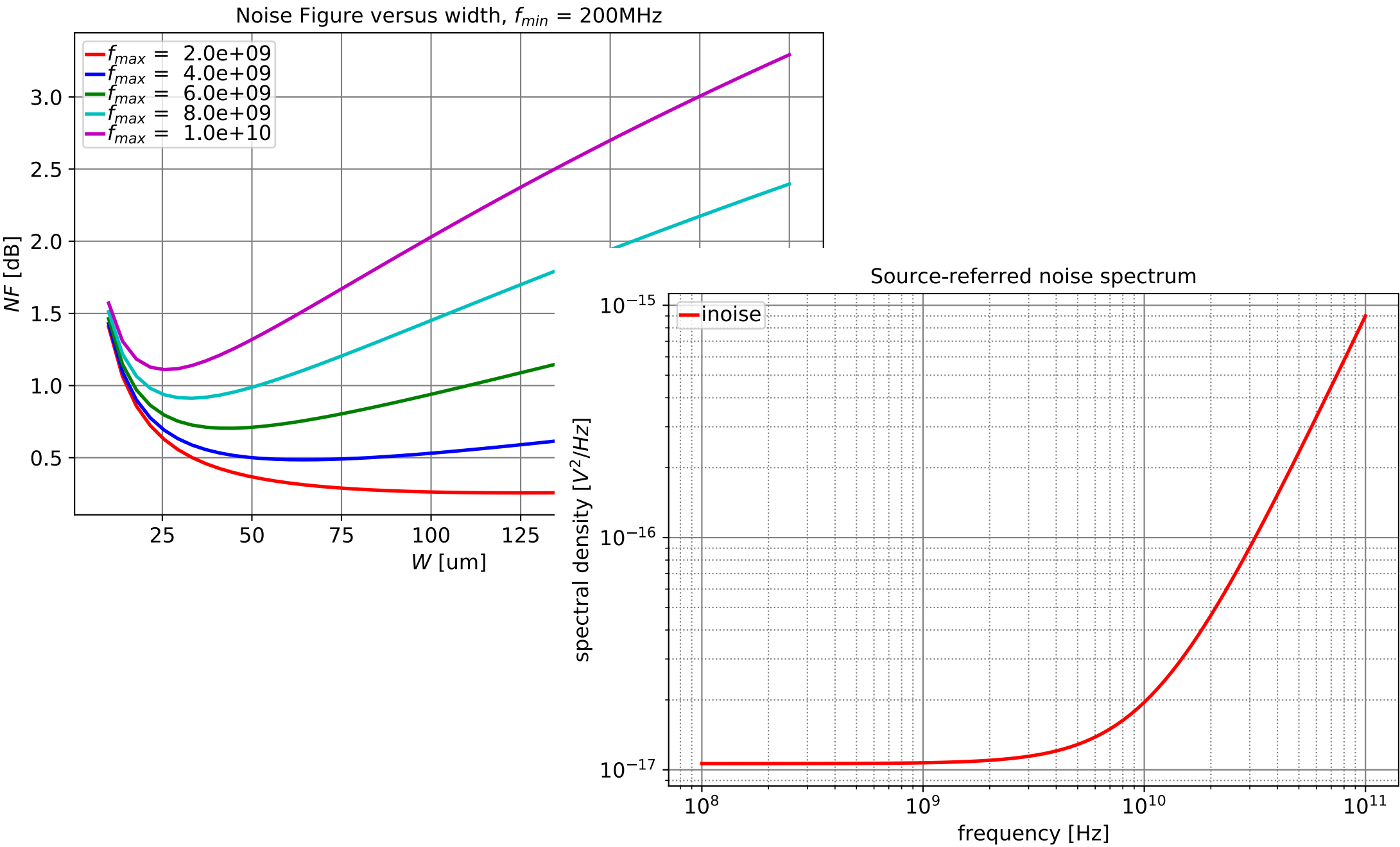
```
"CS stage resistive noise"
* gnetlist -q -g spice-noqsi -o CSresNoise.net CSresNoise.sch
* SPICE file generated by spice-noqsi version 20130710
* Send requests or bug reports to jpd@noqsi.com
.INCLUDE SLICAP.lib
X1 1 0 out NM18_noise ID={ID} W={W} L={L} IG={IG}
R1 2 1 {R_s}
V1 2 0 V value=0 dc=0 dcvar=0 noise={4*k*T*R_s}
.param R_s=600 W=54.6u L=180n ID=6.15m IG=0
.end
```

Operating parameters

- Device width:
- $W = 5.46 \cdot 10^{-5}$ (1)
- Drain current for operation at critical inversion:
- $I_D = 0.006169$ (2)
- The effective noise resistance R_N equals:
- $R_N = 52.39$ (3)
- The cut-off frequency f_T equals:
- $f_T = 3.577 \cdot 10^{10}$ (4)

Study noise behavior for various source types

Find design parameters and show stopper values



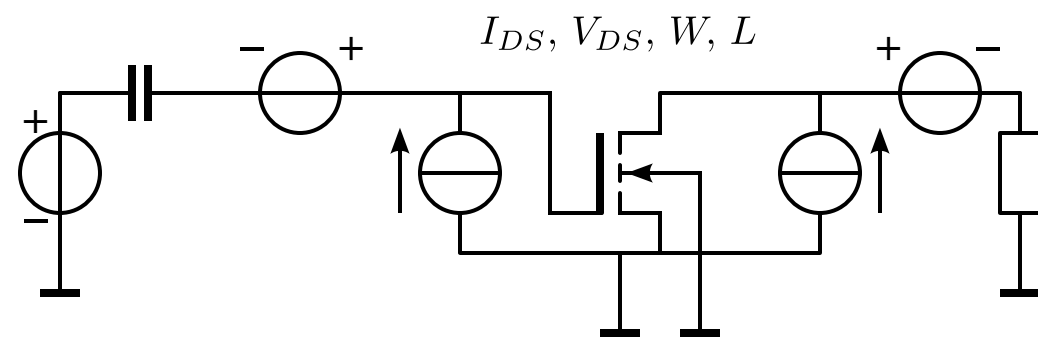
Find design parameters input and output stage

Static and dynamic voltage and current drive capability

Range for drain current, width and length

Noise performance

Range for drain current, voltage, width and length

If overlap, is single-stage solution feasible?

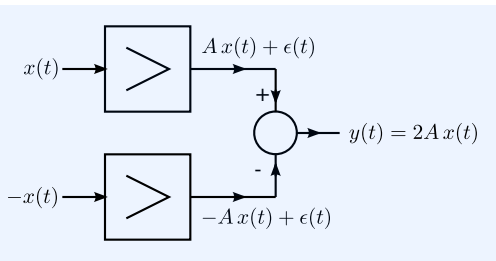
Gain accuracy?
Noise performance?
Drive capability?
Weak nonlinearity?



If OK implement biasing



Balanced CS stages

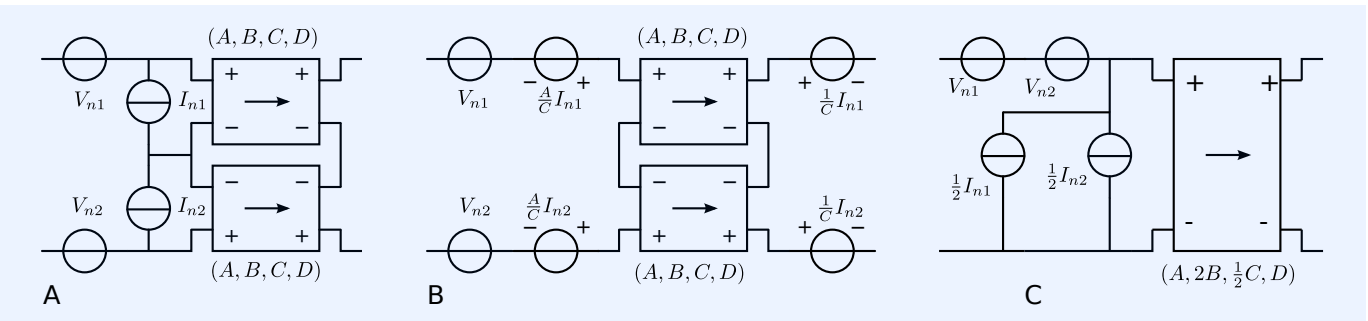
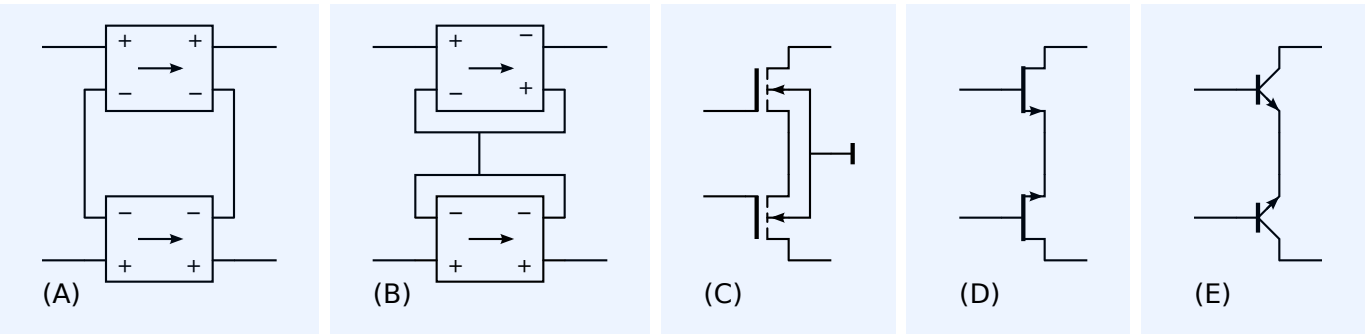
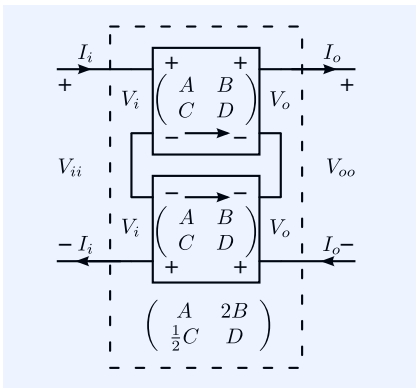


Learn how to generate balanced configurations

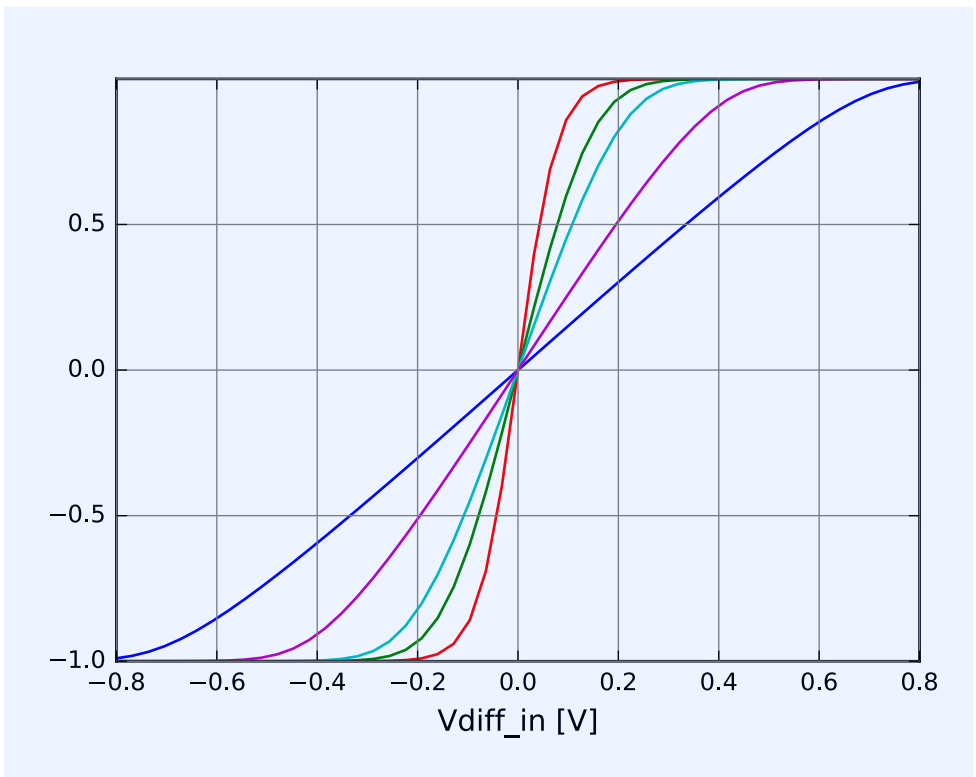
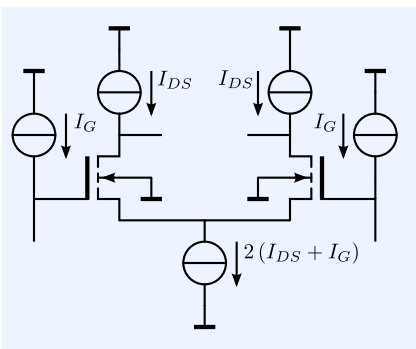
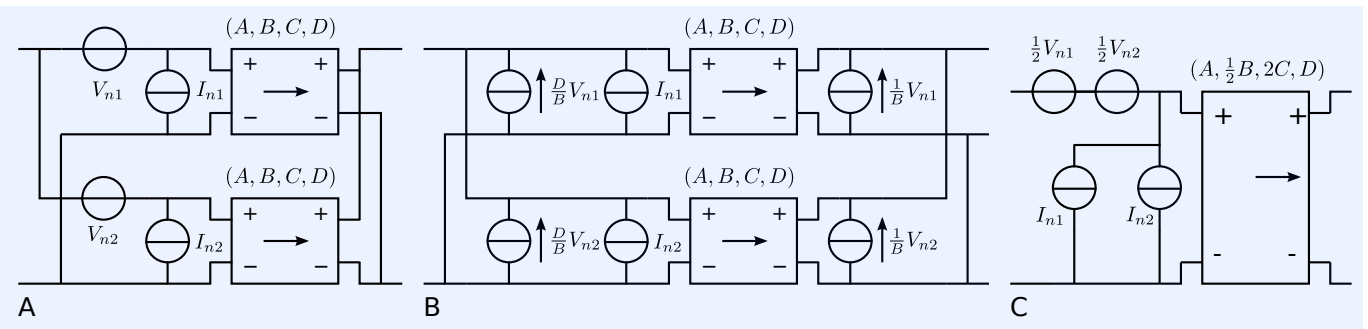
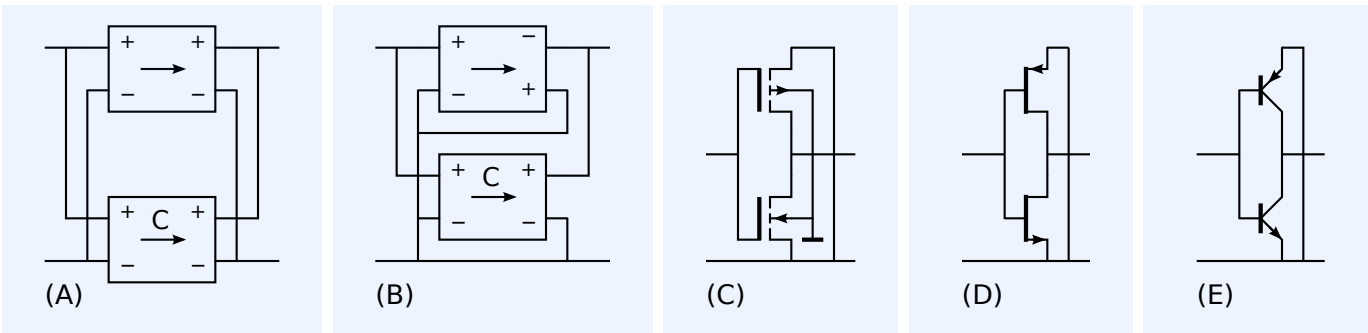
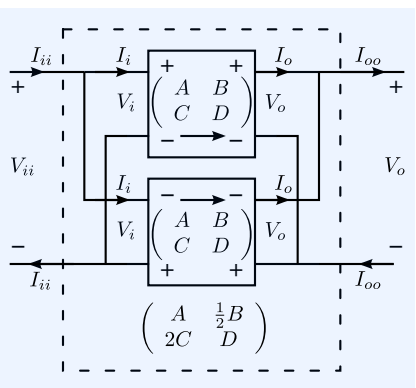
Learn about error-reduction capabilities of balancing

Learn how to relate amplifying capabilities and limitations of balanced configurations to those of unbalanced configurations

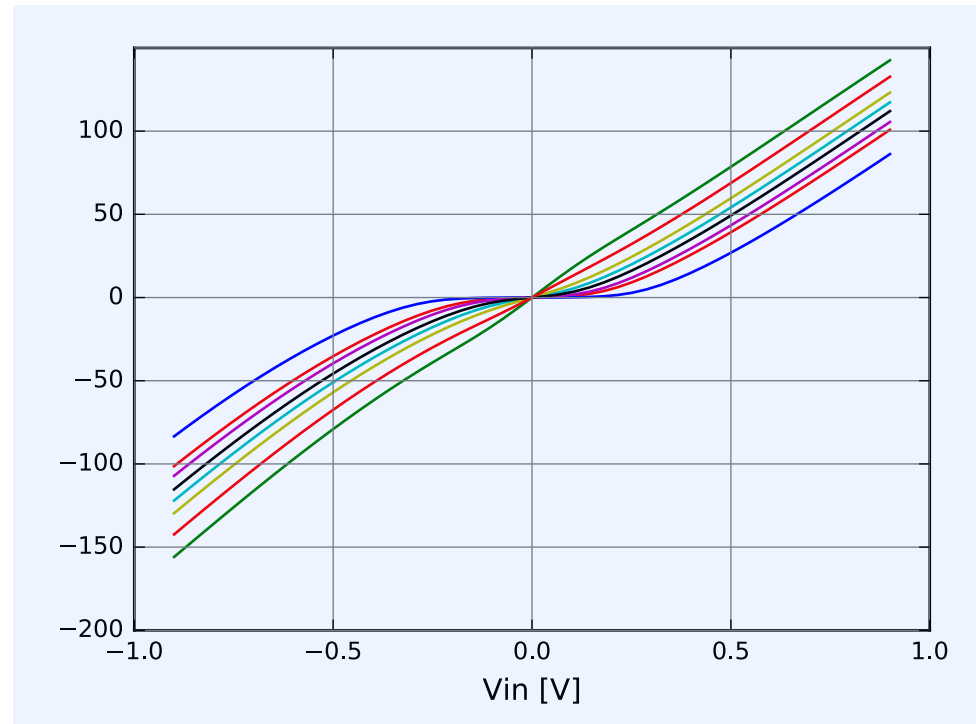
Anti-series connection
Differential pair



Complementary-parallel
connection
Push-pull stage



Compressing odd characteristic

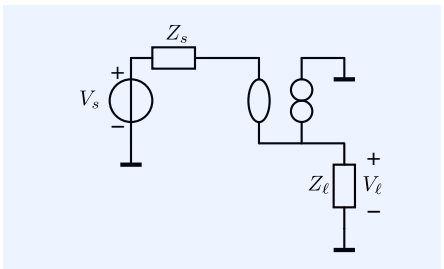
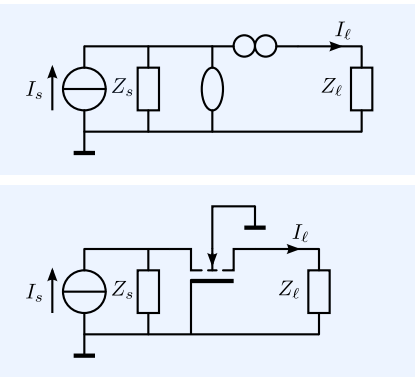
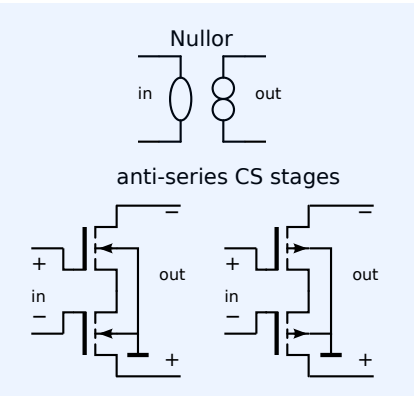
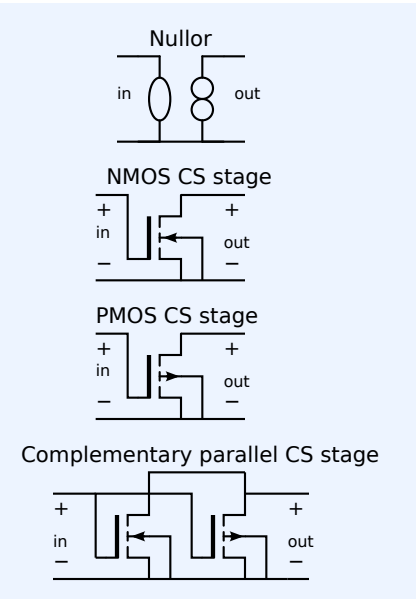


Expanding odd characteristic

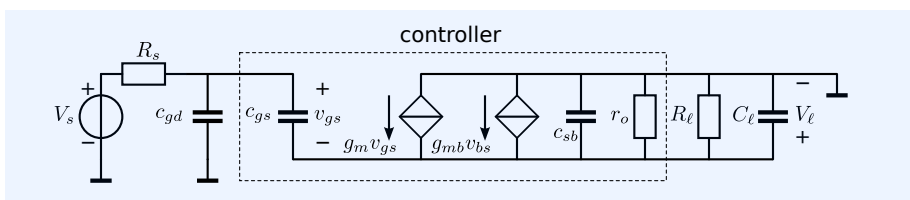
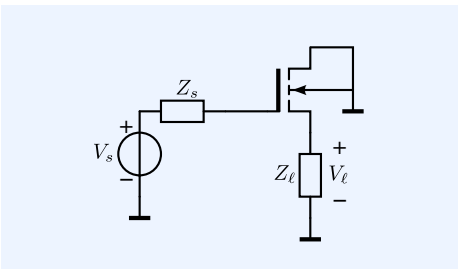
Feedback stages

Learn to predict the behavioral changes resulting from application of negative feedback

Unbalanced or balanced stages applied as controller in feedback amplifiers



Voltage follower (CD stage)

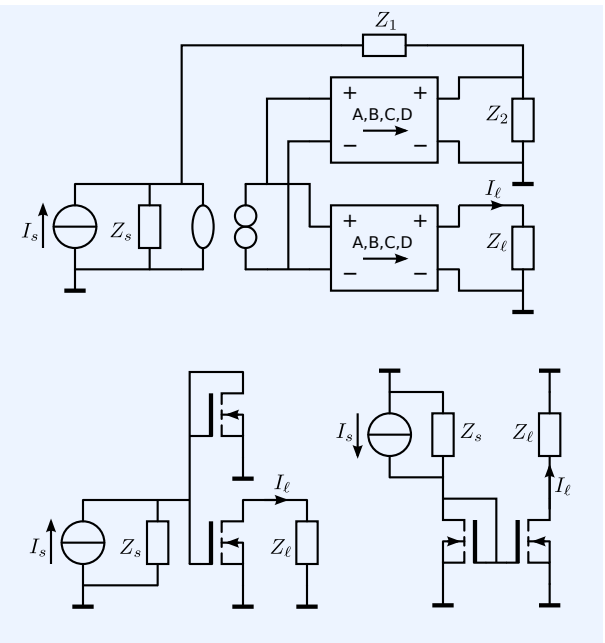


asymptotic-gain feedback model

Bandwidth and phantom-zero compensation

```
>> CDcompM18
GAIN
DC value = 7.281e-01
Poles:
  RealPart  ImagPart  Frequency  Q
  -----
p_1 -9.2226e+08  1.1702e+09  1.49e+09  0.80779
p_2 -9.2226e+08 -1.1702e+09  1.49e+09  0.80779
Zeros:
  RealPart  ImagPart  Frequency  Q
  -----
z_1 -1.3667e+10  0  1.3667e+10  0
>>
```

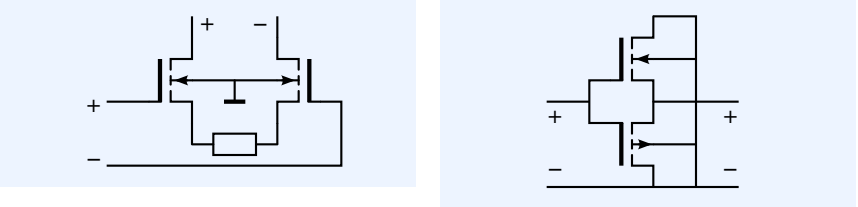
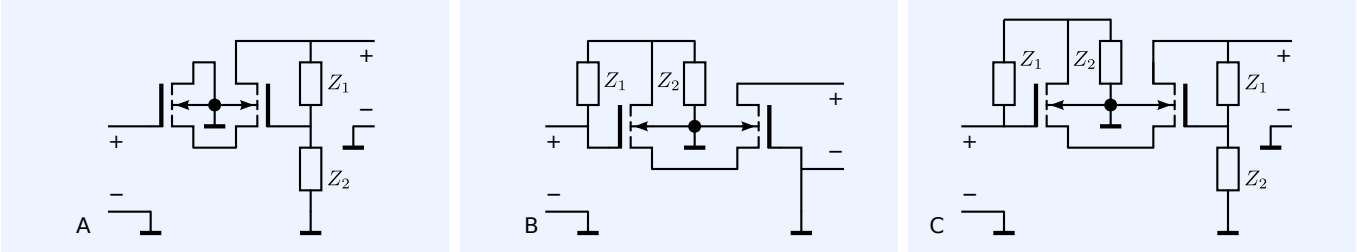
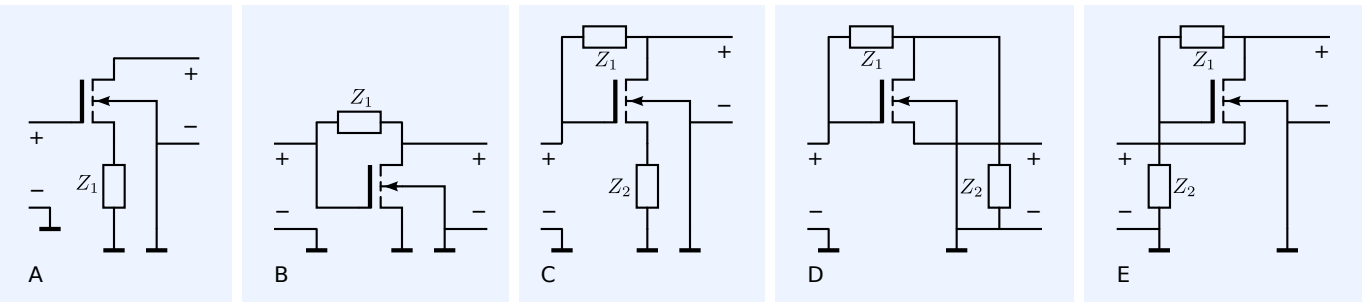
Indirect feedback stages
Current mirror



Passive feedback stages; unbalanced controller

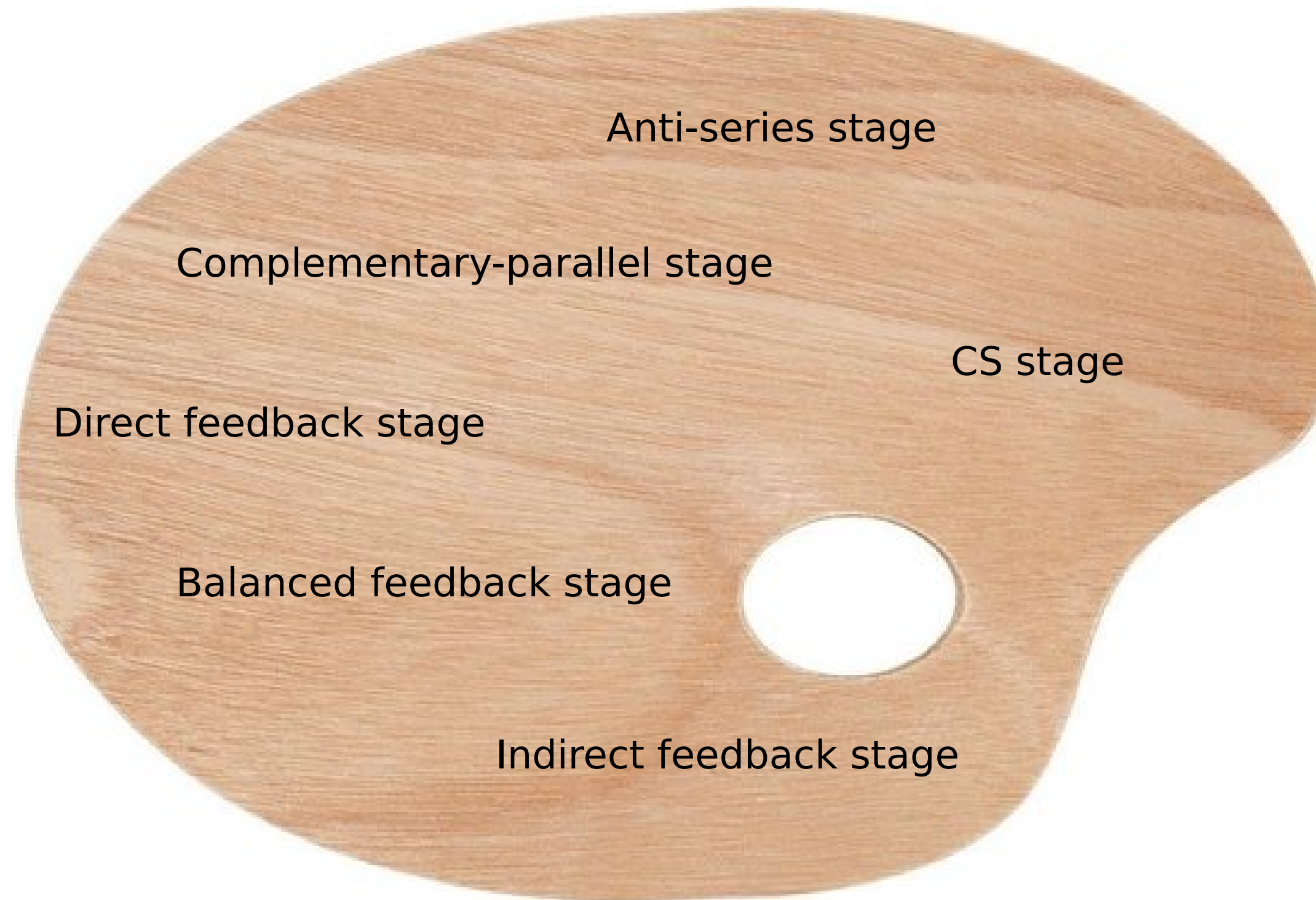
Passive feedback stages; balanced controller

Balanced feedback stages



Multiple-stage active antenna

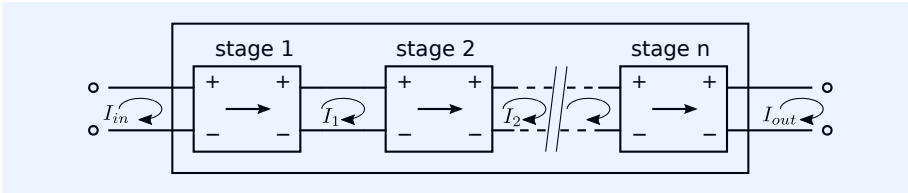
Cascade connection of various types of stages



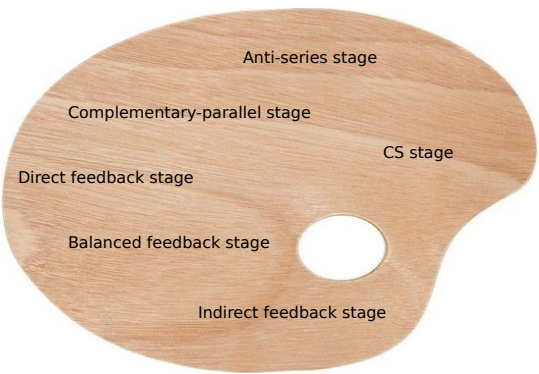
Feedback amplifiers with multiple-stage controller

How many stages?
$$n = \frac{m \log f_H - \log LP_1}{\log \frac{f_T}{f_H}}$$

How to interconnect the stages?



What type of stages?

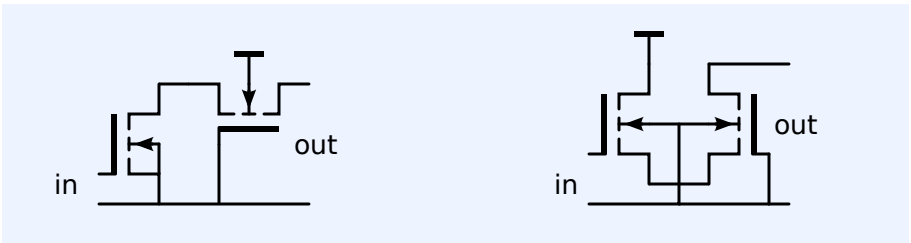


What type of input stage?

What type of output stage?

What type of intermediate stages?

How to reduce the interaction between stages?



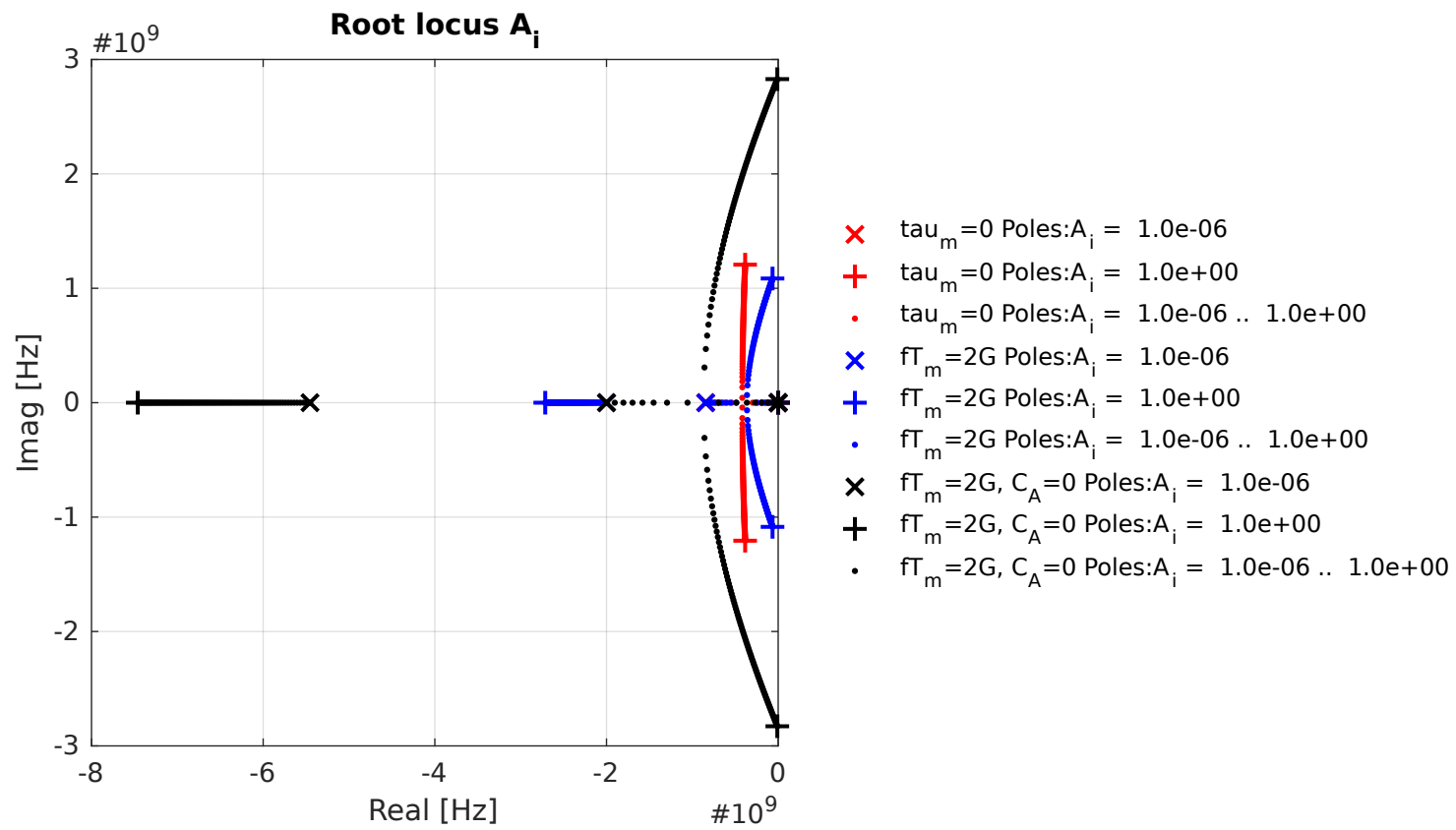
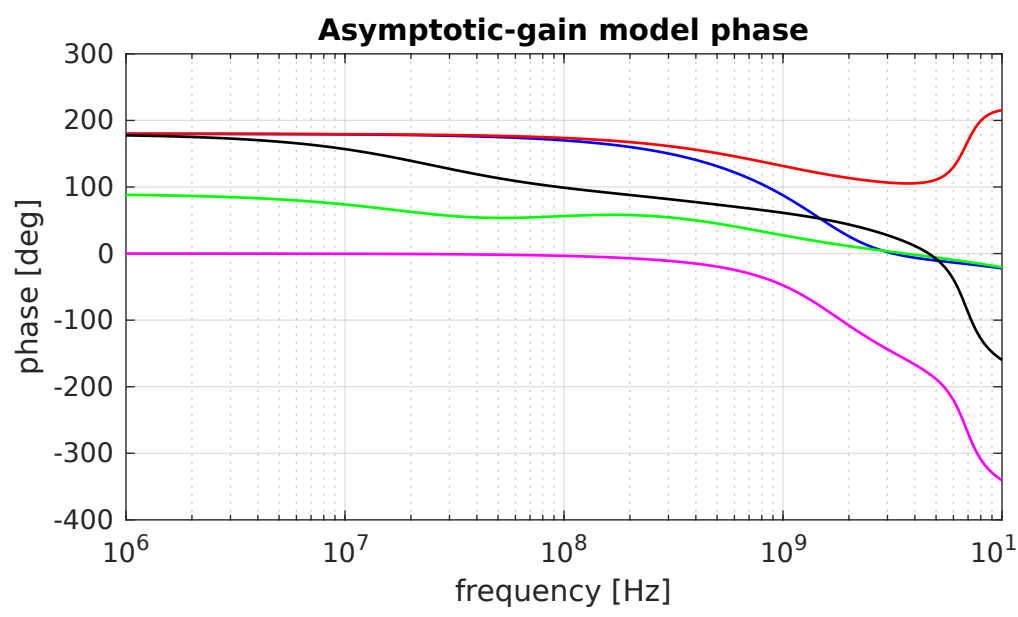
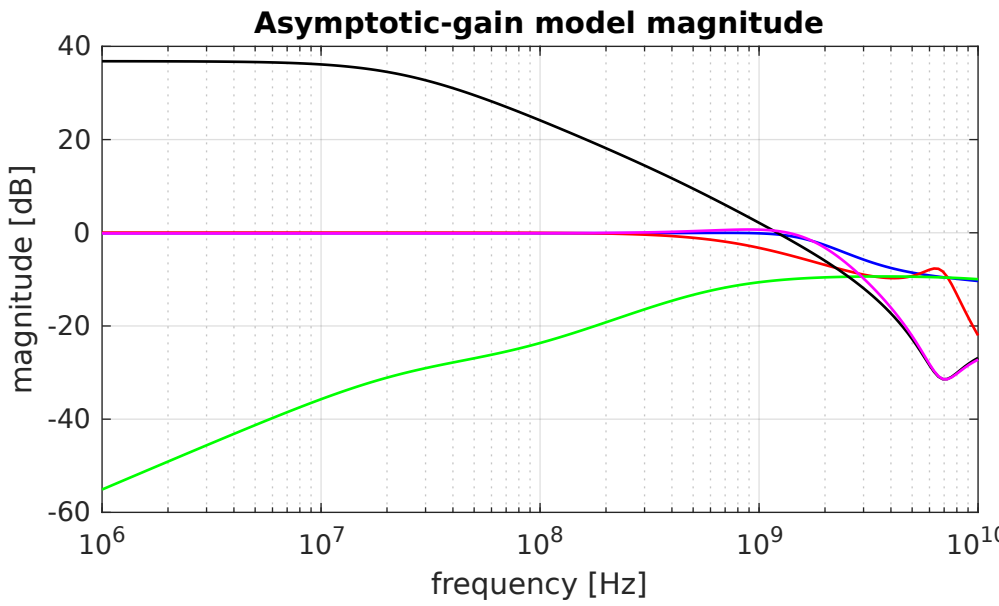
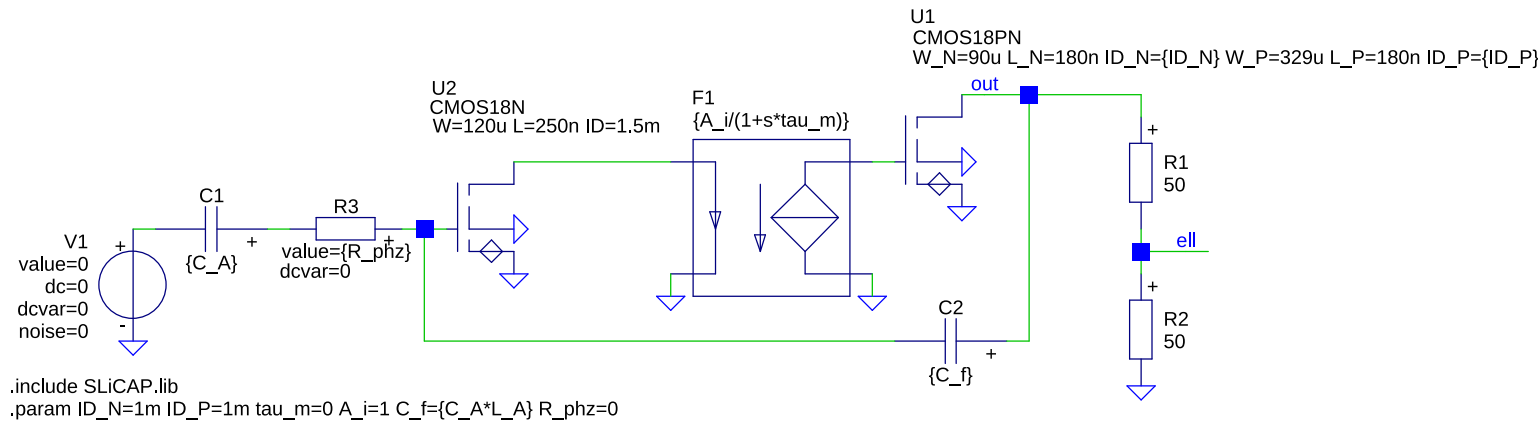
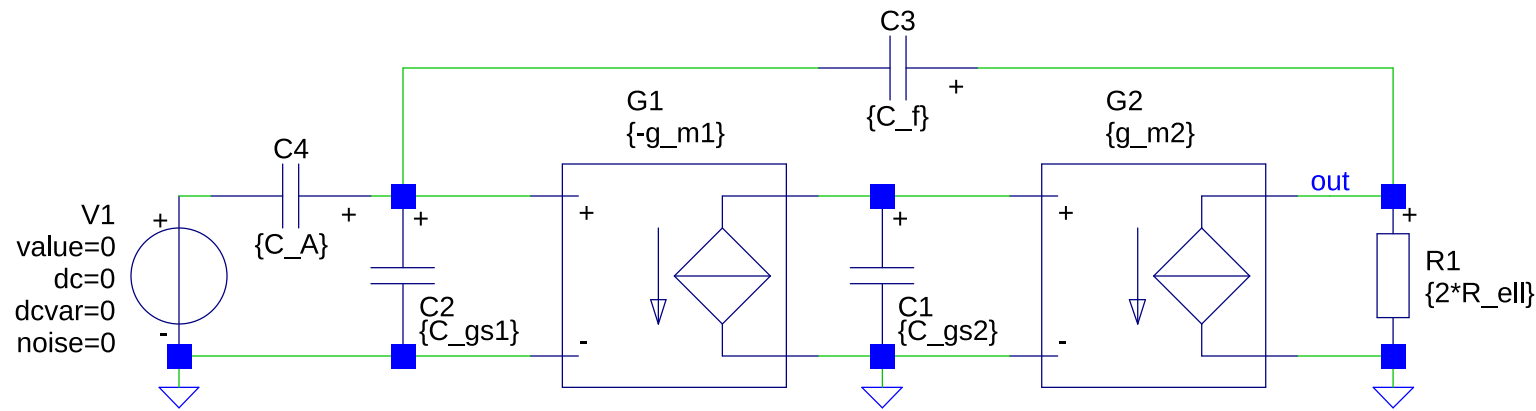
Maximization of contribution to loop gain-poles product
Minimization of Miller effect

Stepwise design of

Drive capability

Noise performance

Bandwidth



Phantom zero compensation

Recap of concept EE3C11
Application in transistor circuits

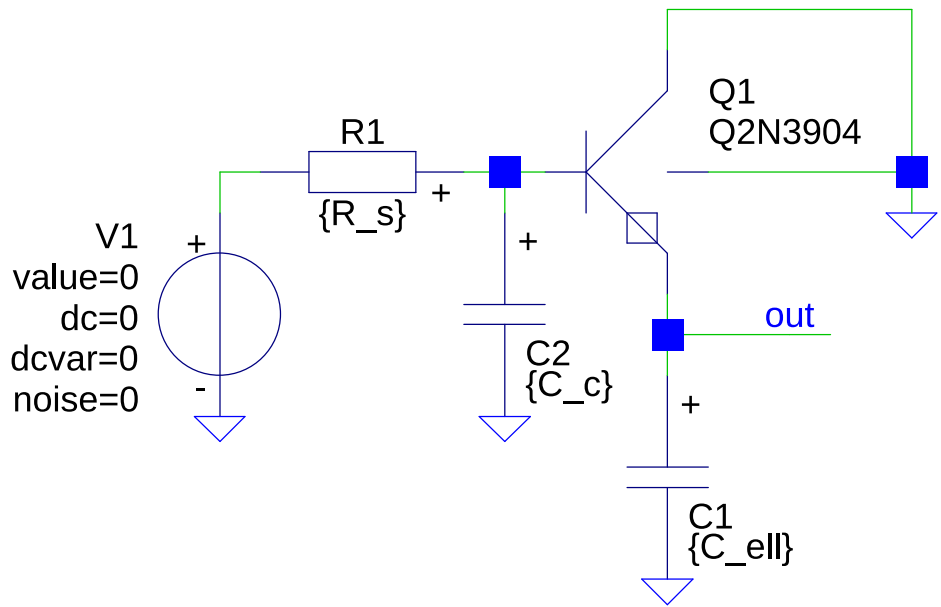
Pole-splitting

"Miller compensation"

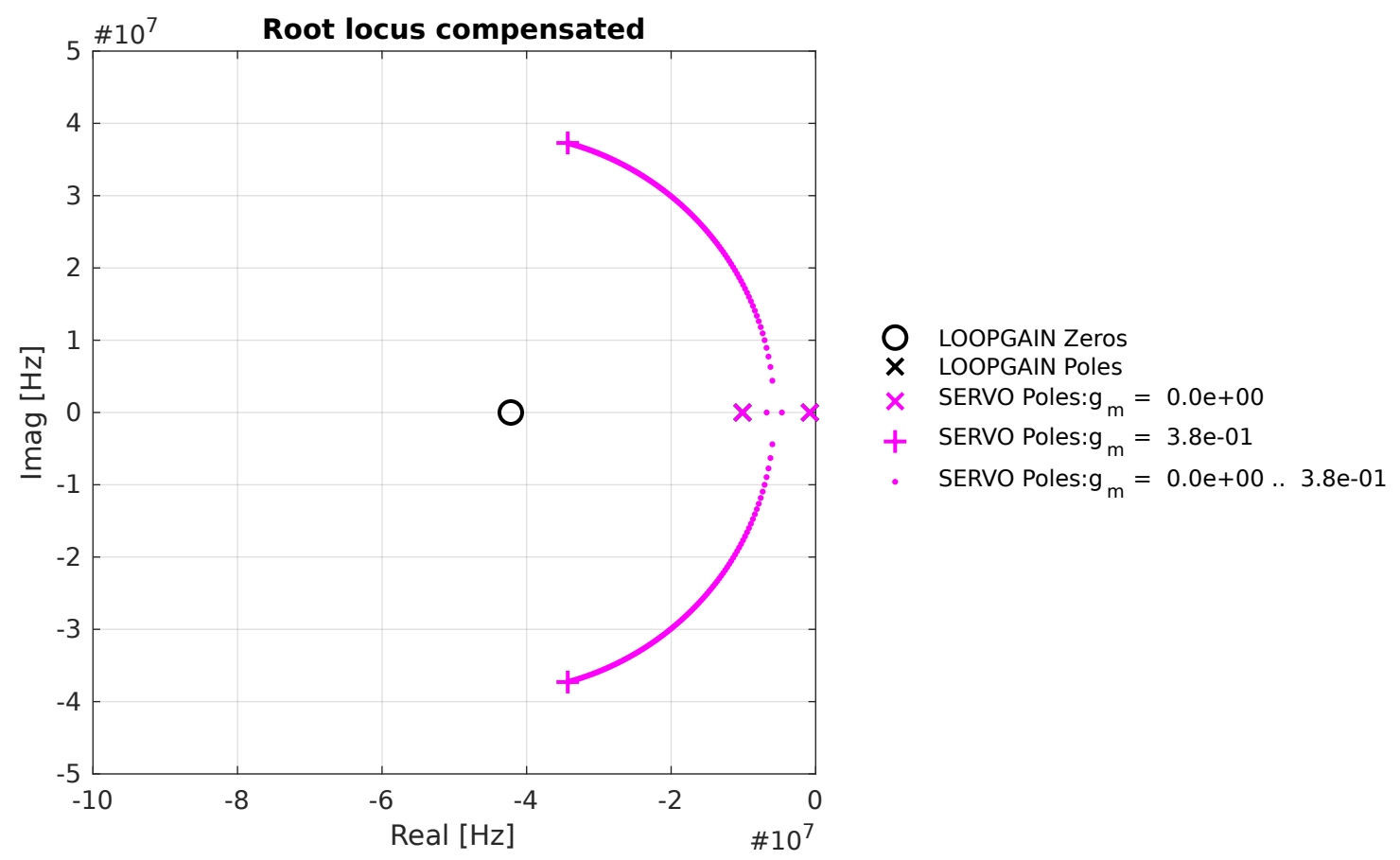
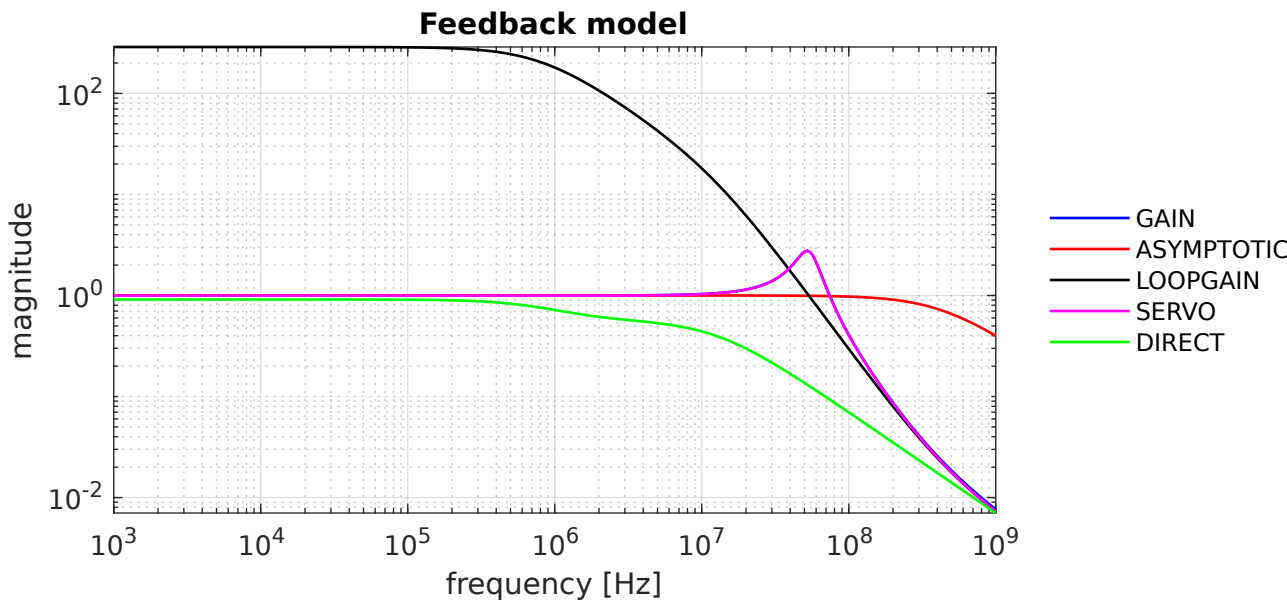
Pole-zero canceling

Resistive broadbanding

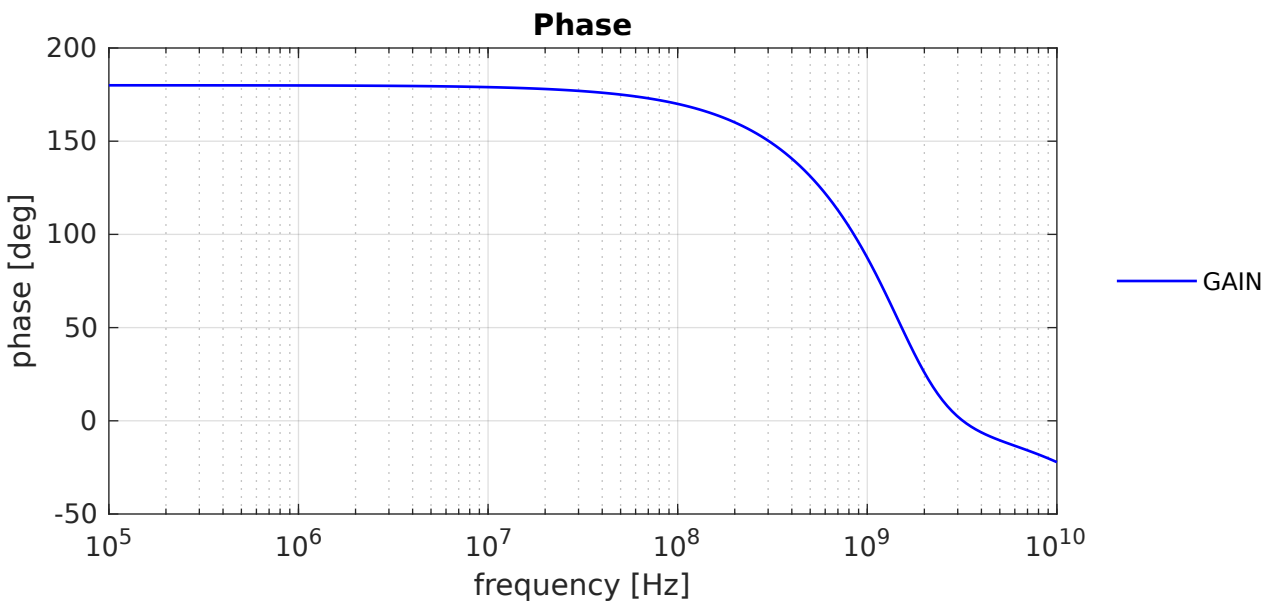
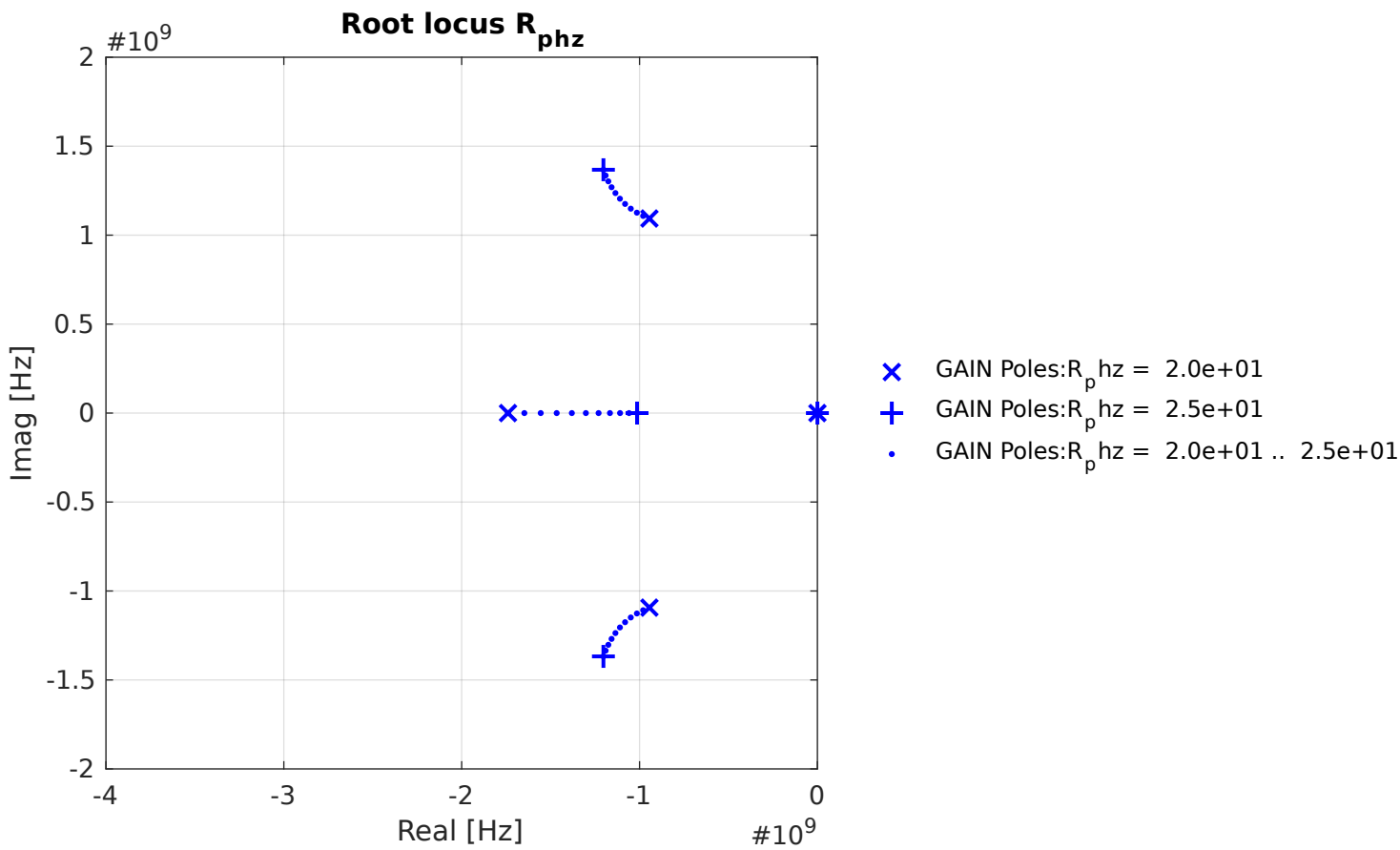
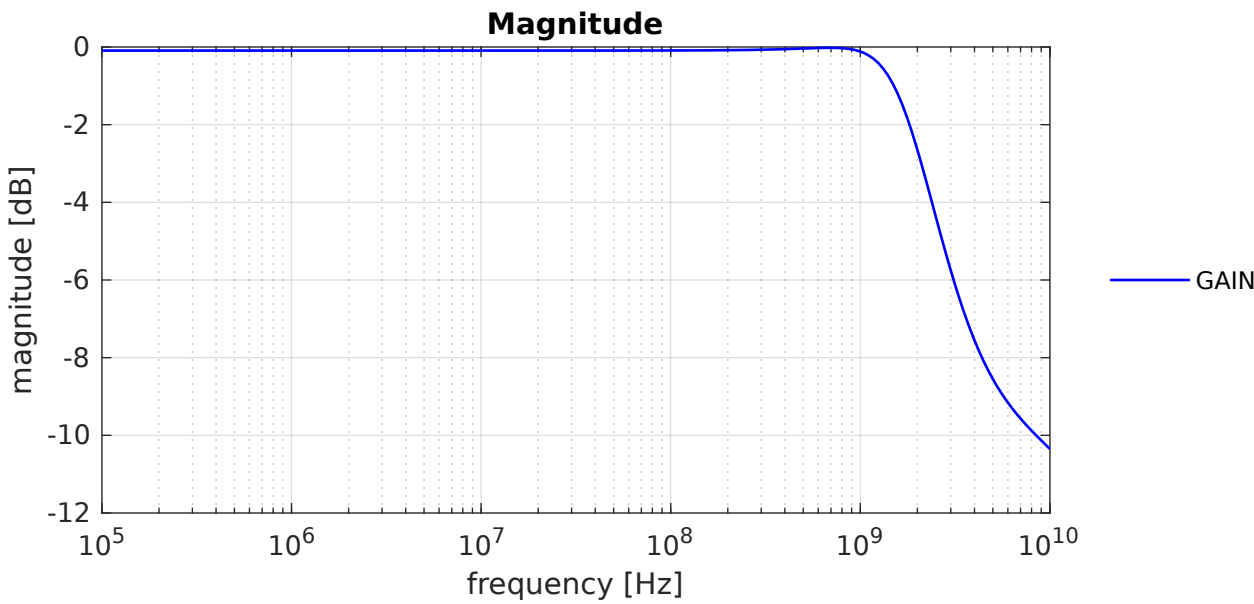
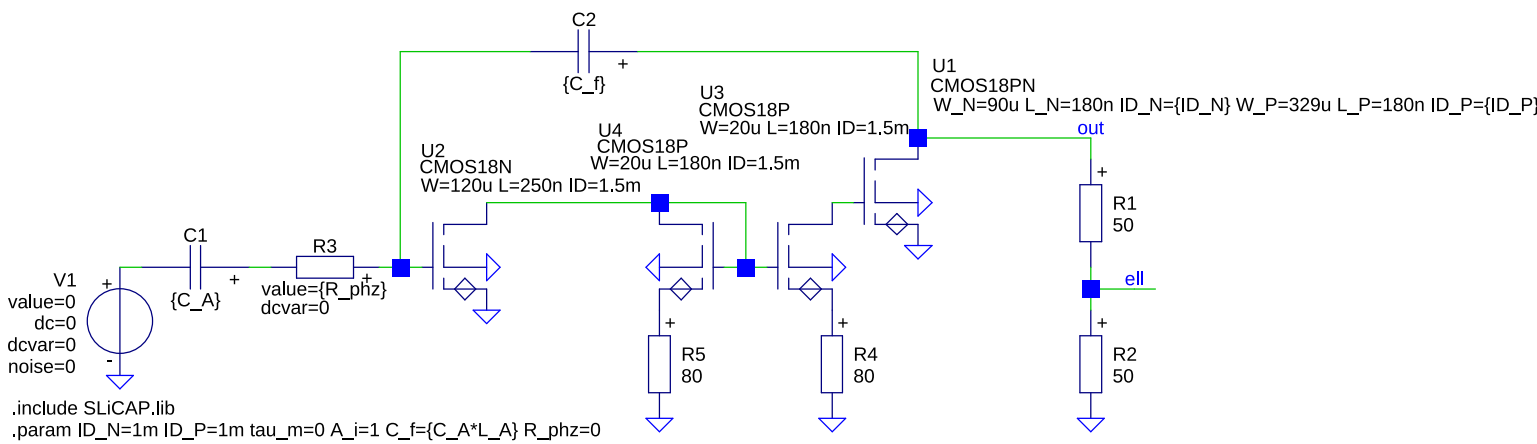
Bandwidth limitation



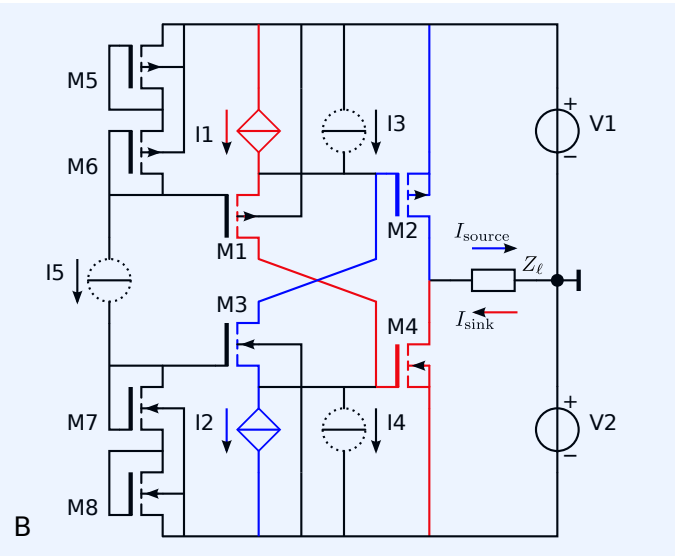
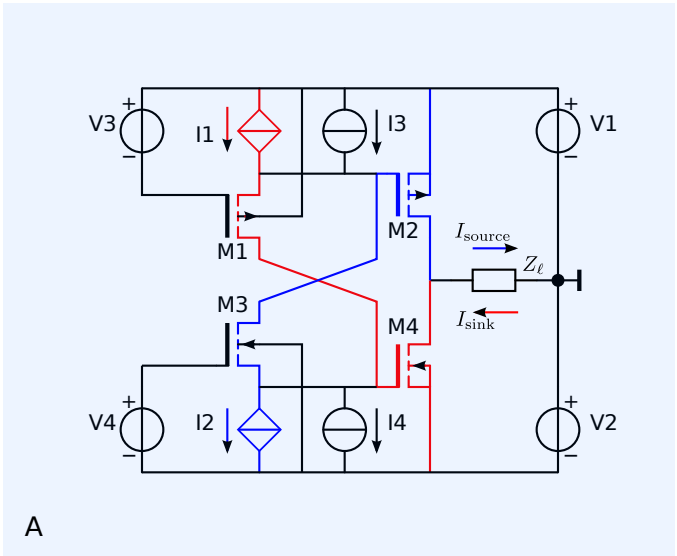
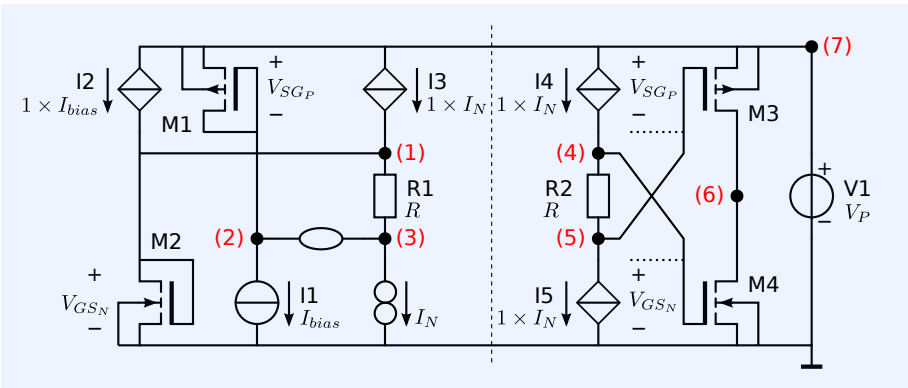
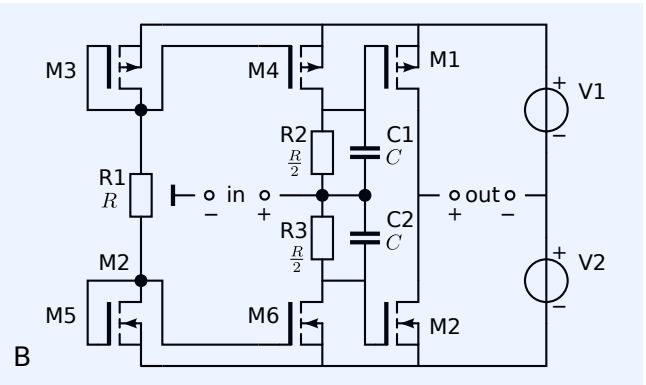
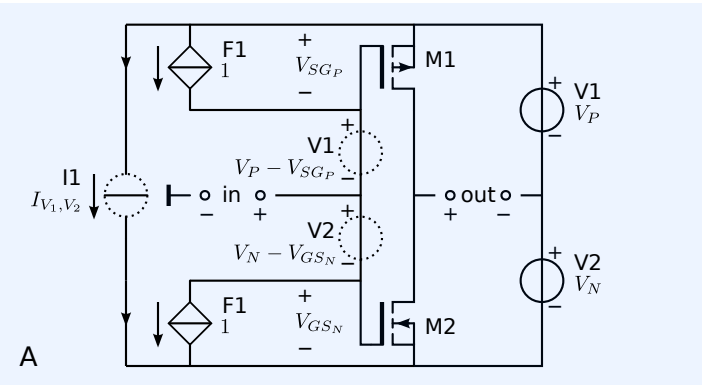
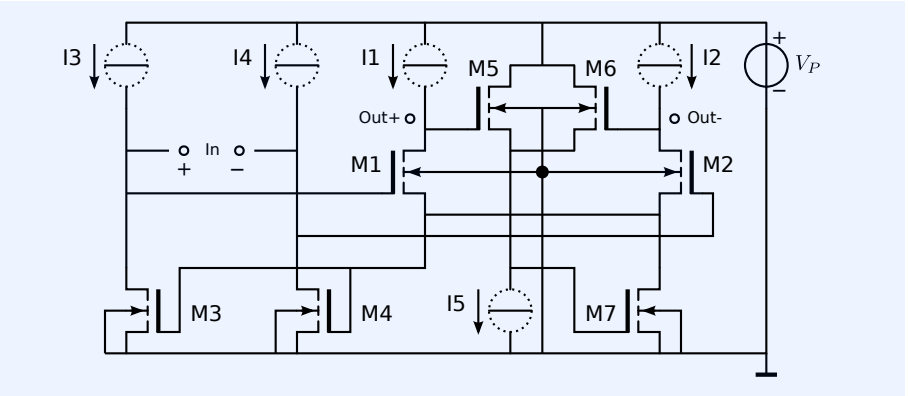
```
.model Q2N3904 QV gpi={g_m/beta_AC} gm={g_m} go={g_o} rb={r_b} cpi={c_pi} cbc={c_bc}
.param g_m=377m beta_AC=323 r_b=20 c_pi=145p c_bc=1.7p g_o=90.9u
.param R_s=200 C_ell=100p C_c=0
```



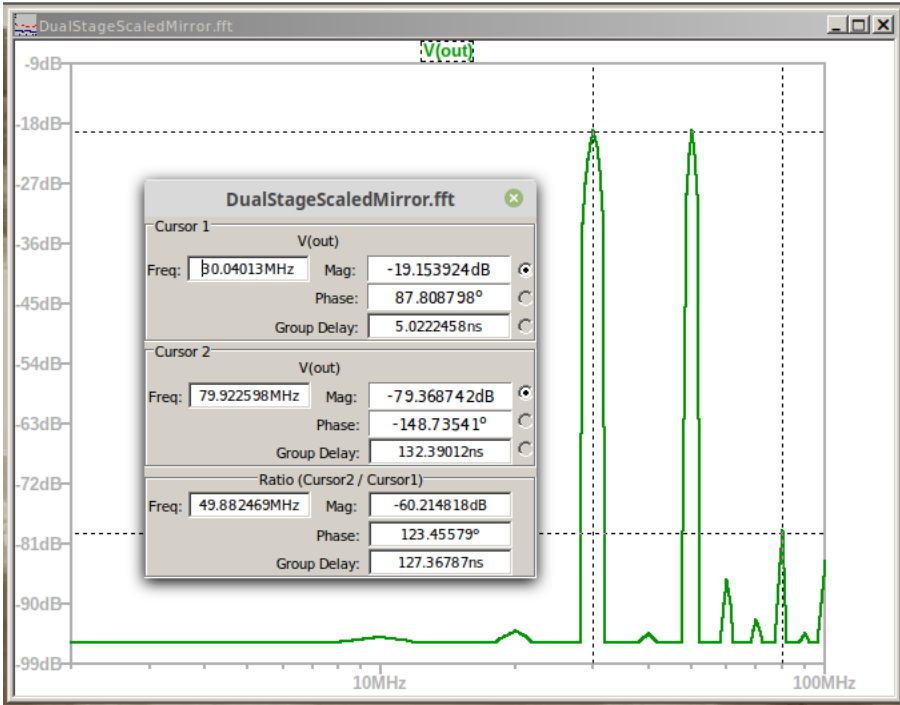
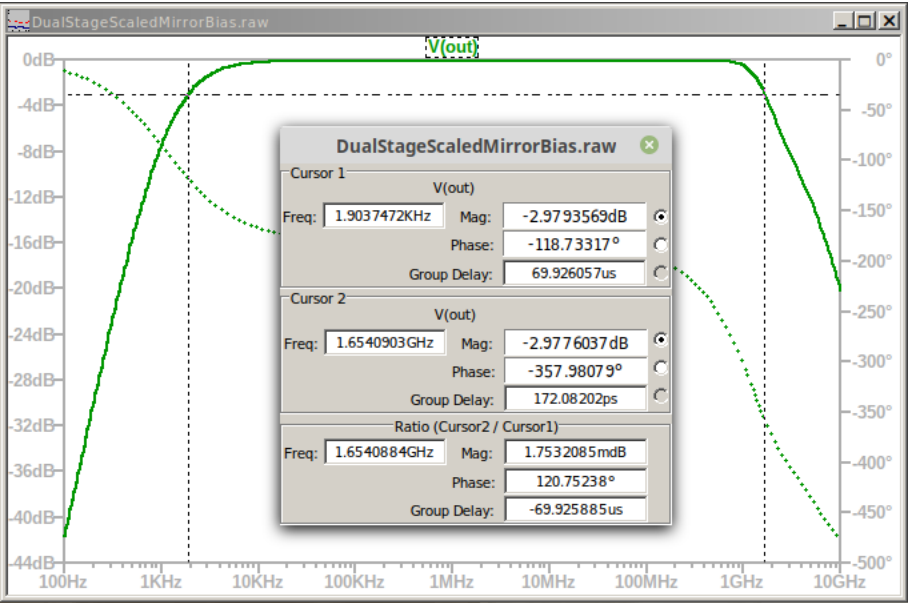
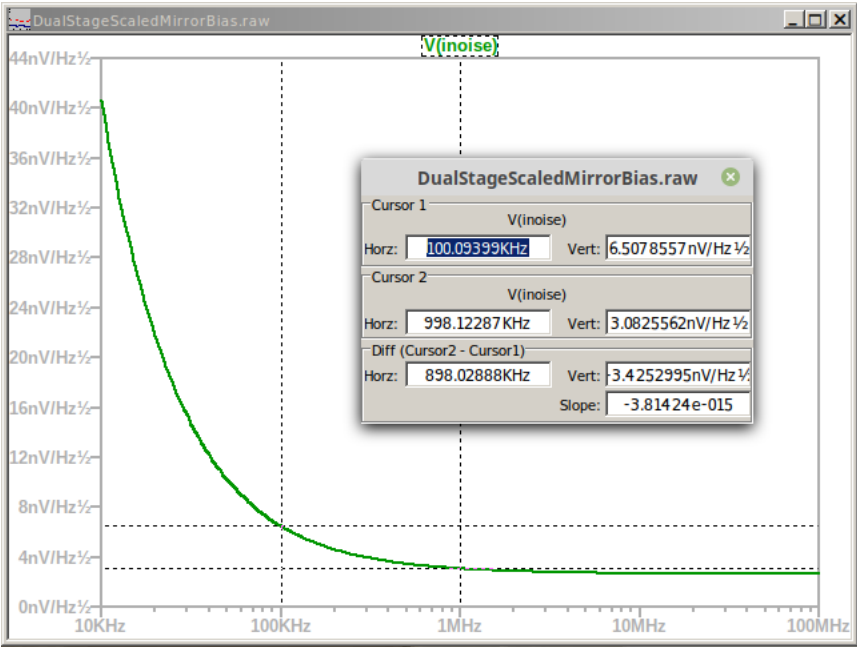
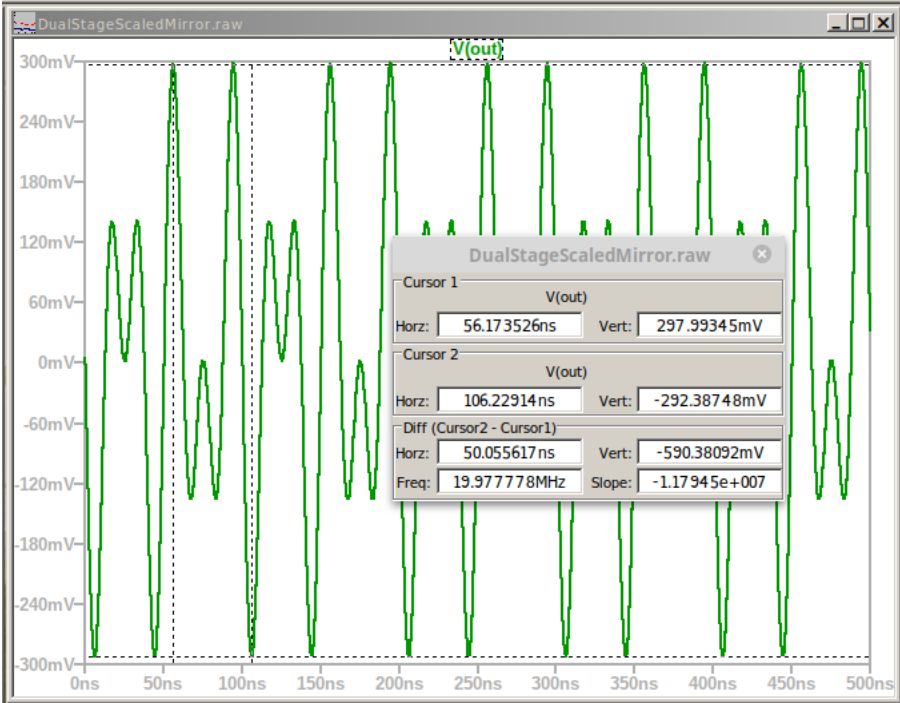
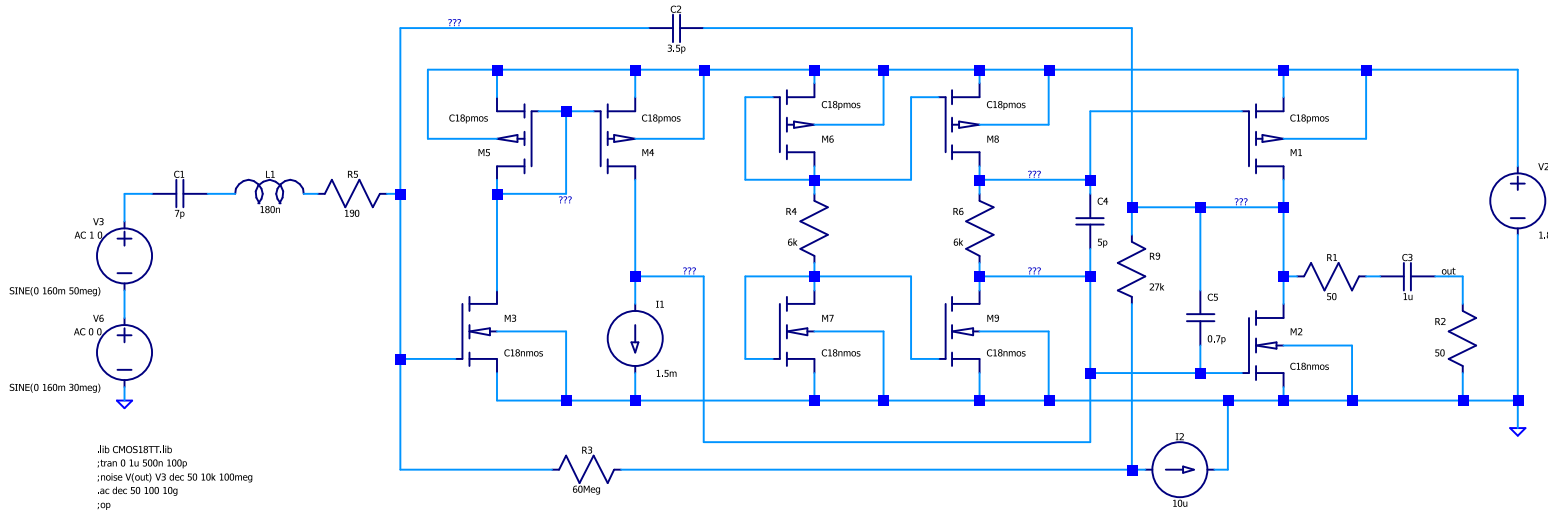
Active antenna design frequency response



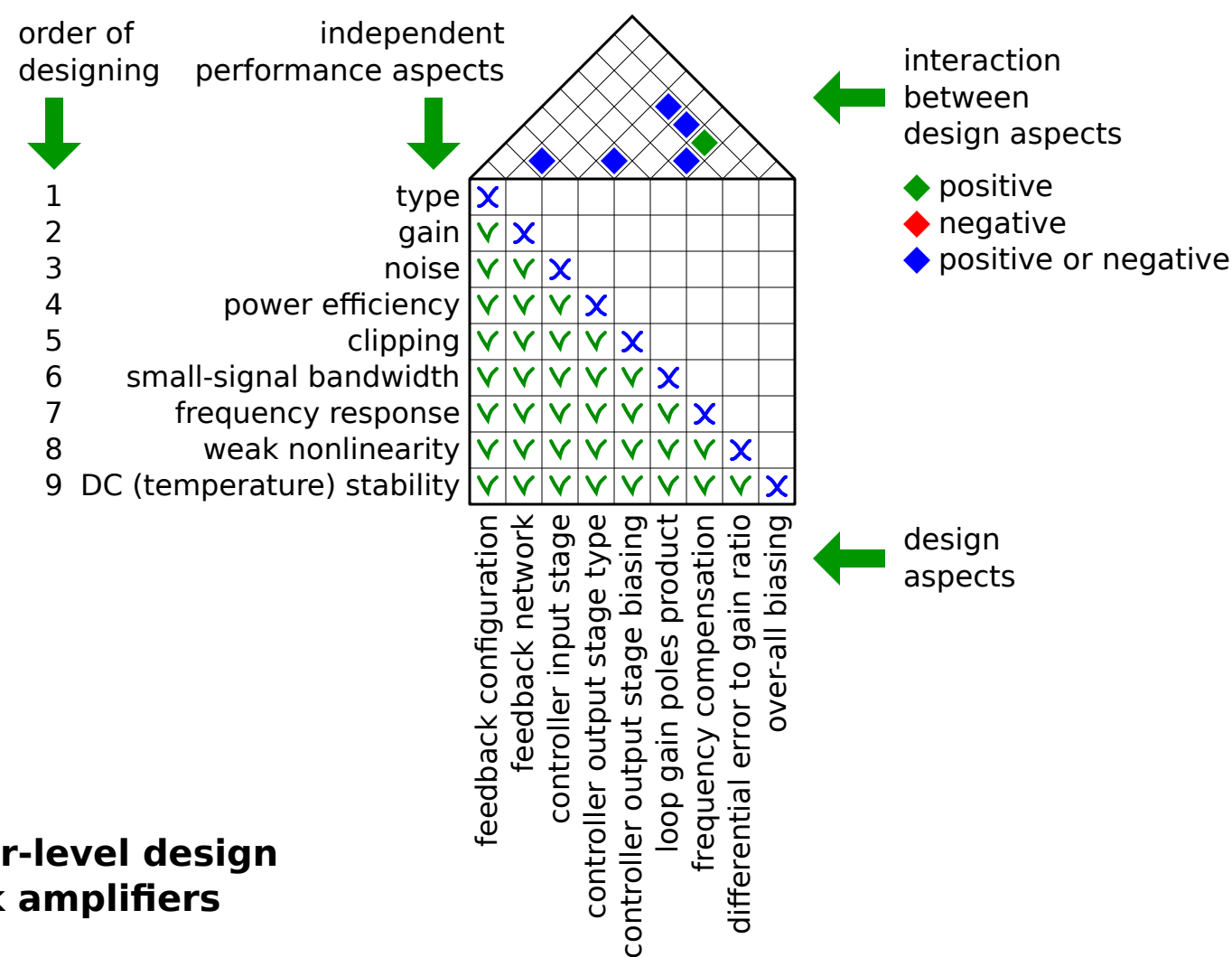
- Design of biasing concepts
- Minimization of floating voltage sources
- Common mode biasing
- Implementation of bias sources
- Evaluation of biasing errors
- Application of error reduction techniques



Completion design active antenna



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an application of:
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Function
Deployment



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Design sequence and
flow chart amplifier design

**Orthogonal transistor-level design
of negative feedback amplifiers**