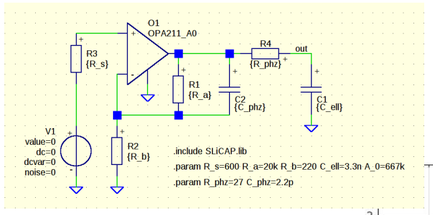
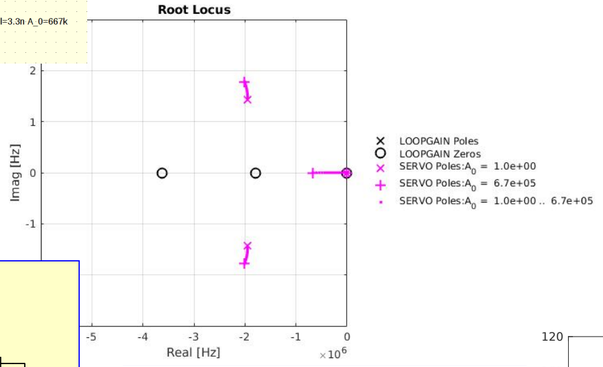
# EE3C11: Structured Electronic Design
# My First Voltage Amplifier
# Design example EE3C11




SLiCAP project: myFirstVamp

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5. myFirstVampOPA211completeNoise

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SLiCAP: Symbolic Linear Circuit Analysis Program, Version 0.6 © 2009-2019 Anton Montagne

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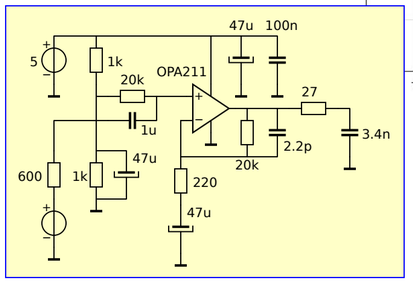
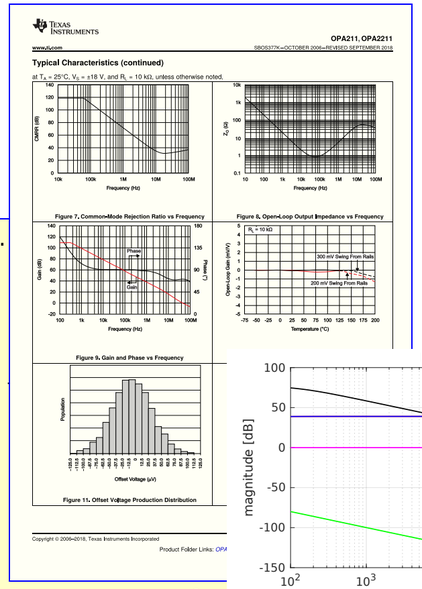
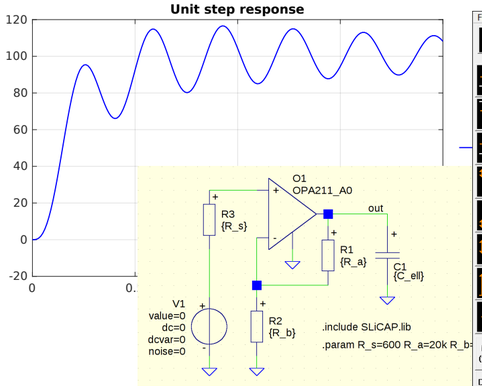
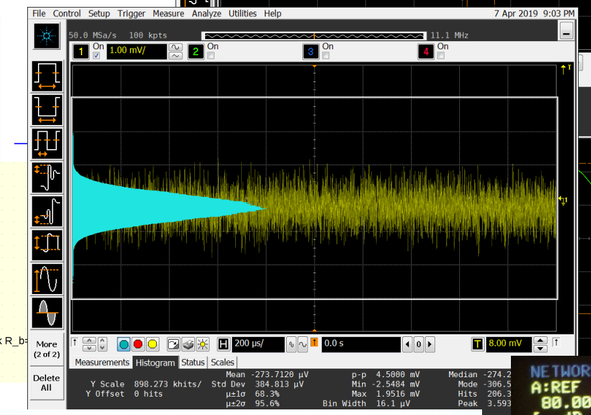


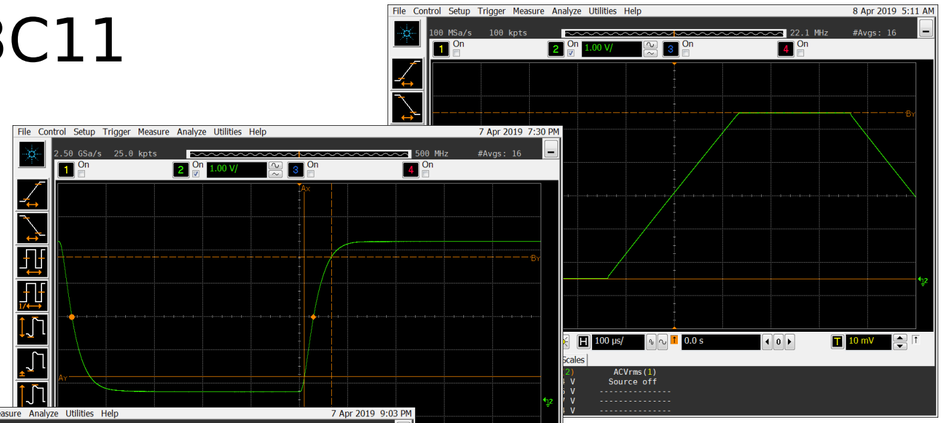









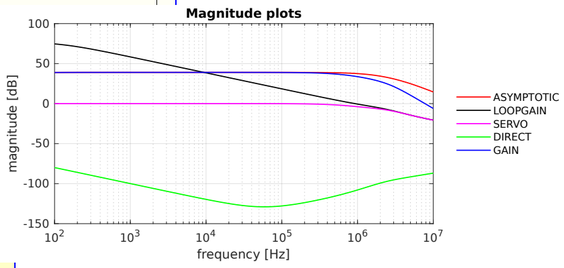




```
Checking circuit: myFirstVampCompensated.
No errors found!
    GAIN
    DC value = 9.189e+01
    Poles:
```

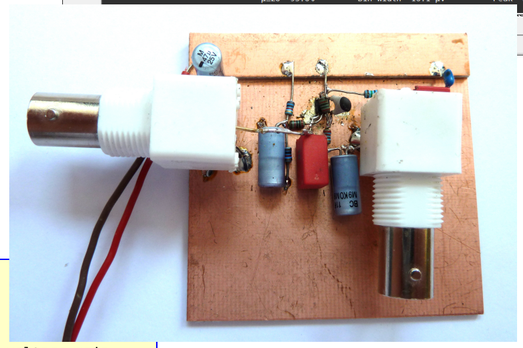
| | RealPart | ImagPart |
|---|---|---|
| p_1 | -7.8738e+05 | 0 |
| p_2 | -1.6015e+06 | 1.9166e+06 |
| p_3 | -1.6015e+06 | -1.9166e+06 |
| p_4 | -1.9604e+07 | 0 |
| p_5 | -2.383e+07 | 0 |
| p_6 | -5.0504e+08 | 0 |

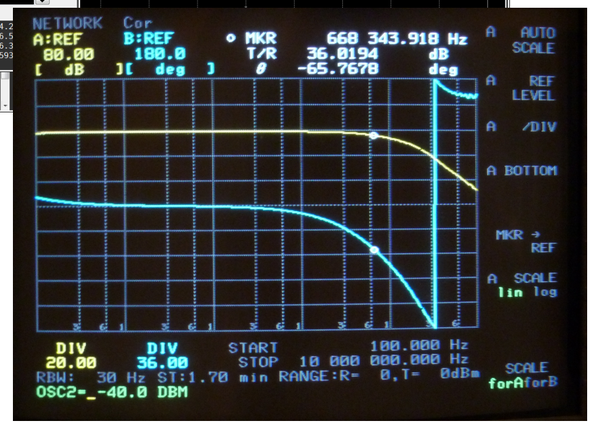
Zeros:

| | RealPart | ImagPart | Frequency | Q |
|---|---|---|---|---|
| z_1 | -1.061e+07 | 0 | 1.061e+07 | 0 |
| z_2 | -3.9963e+07 | 0 | 3.9963e+07 | 0 |
| z_3 | -8.0941e+08 | -7.4266e+08 | 1.0985e+09 | 0.67858 |
| z_4 | -8.0941e+08 | 7.4266e+08 | 1.0985e+09 | 0.67858 |




```
.model OPA211_A0 OV
+ cd = 8p  ; differential-mode input capacitance
+ gd = 50u ; differential-mode input conductance
+ cc = 2p  ; common-mode input capacitance
+ av = {A_0*(1+s/2/PI/40M)/(1+s/2/PI/120)/(1+s/2/PI/20M)}   ; voltage gain
+ zo = {3.6k/(1+s*3.6k*8u) + 0.7 + s*900n*60/(60+s*900n)}   ; output impedance
```





# Application and initial specification

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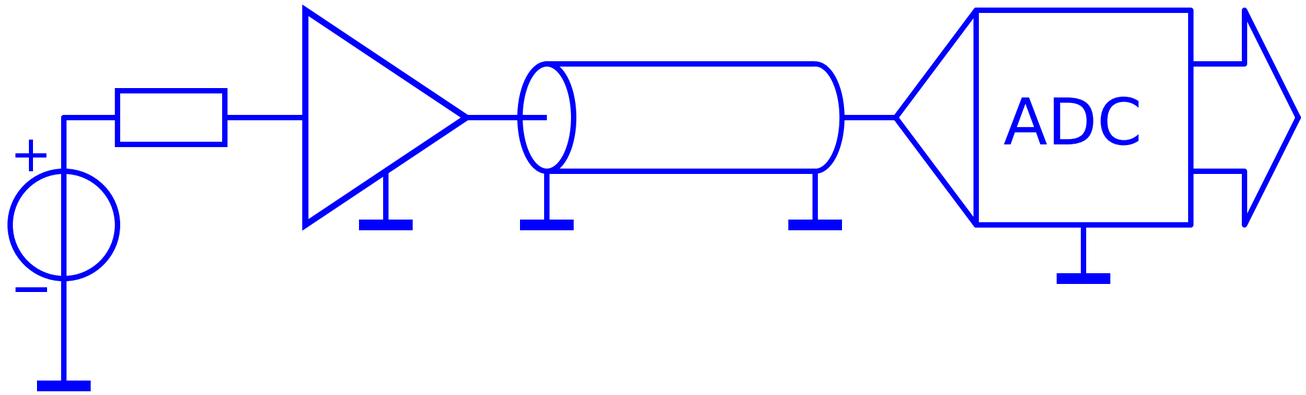


 

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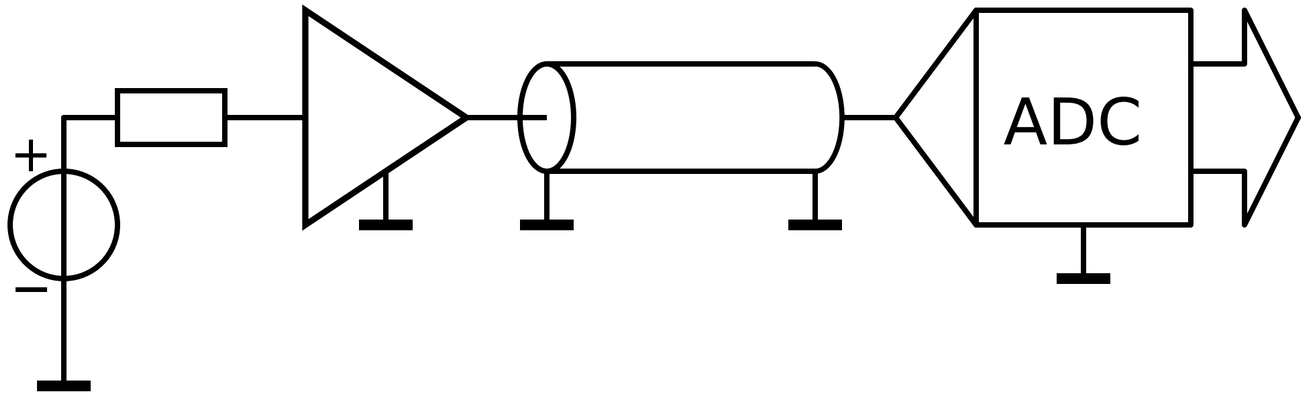


Signal source: voltage, mean value=0, max. deviation +/- 25mV$_p$

 

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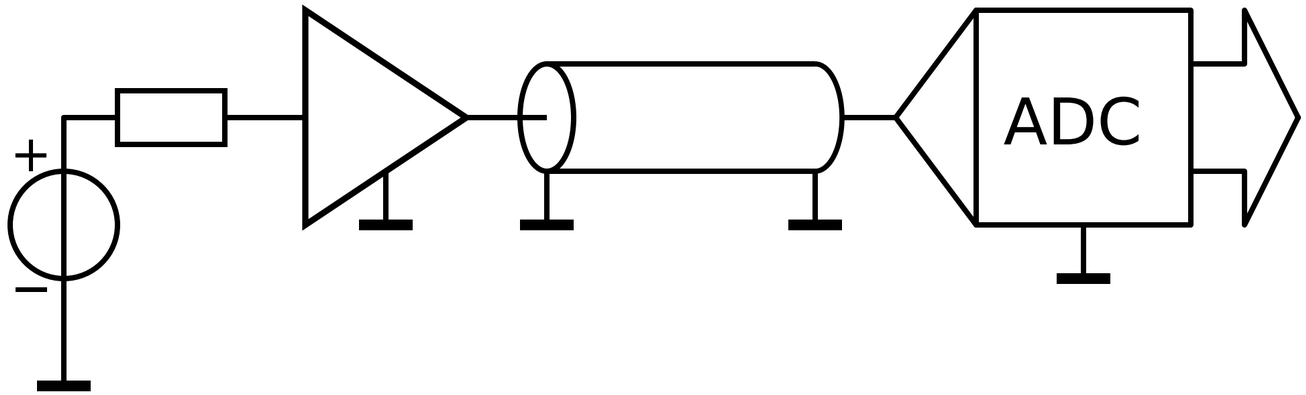


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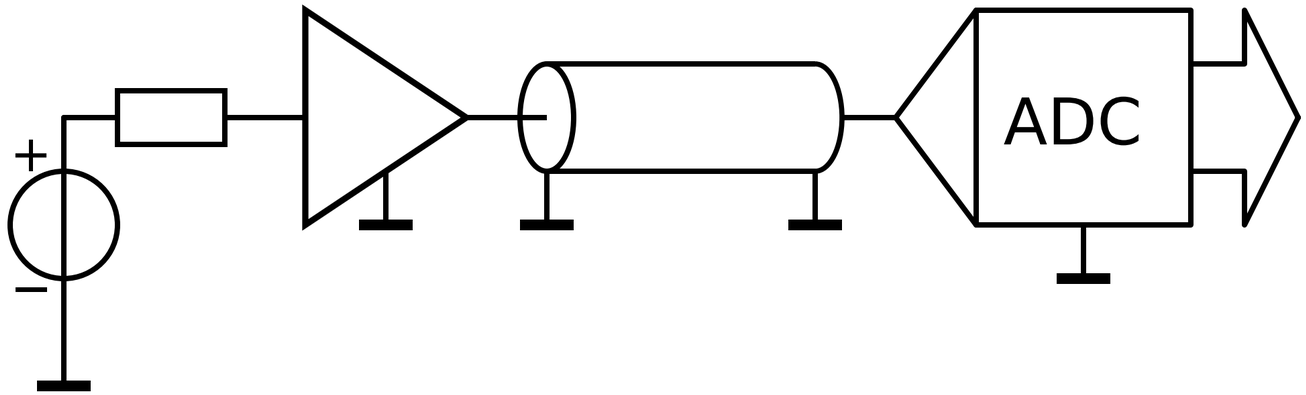


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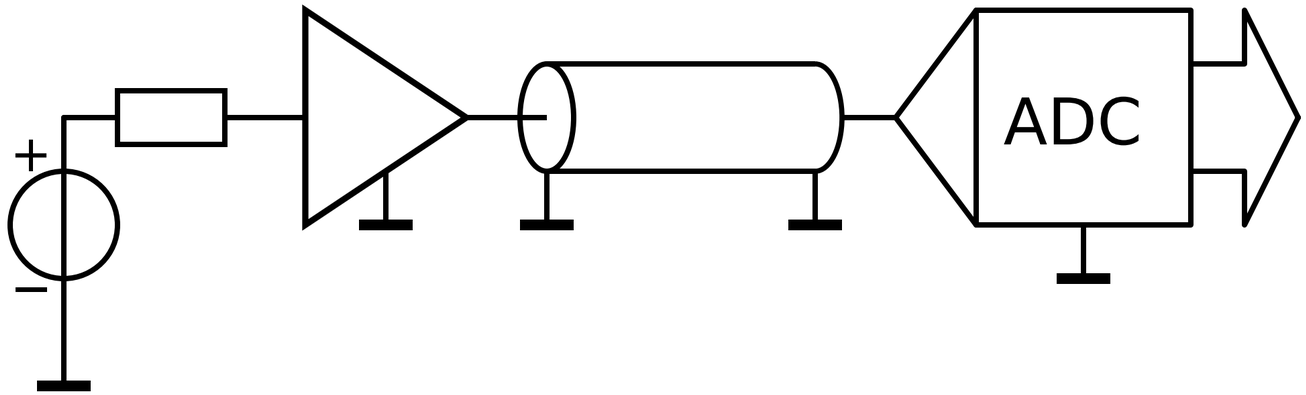


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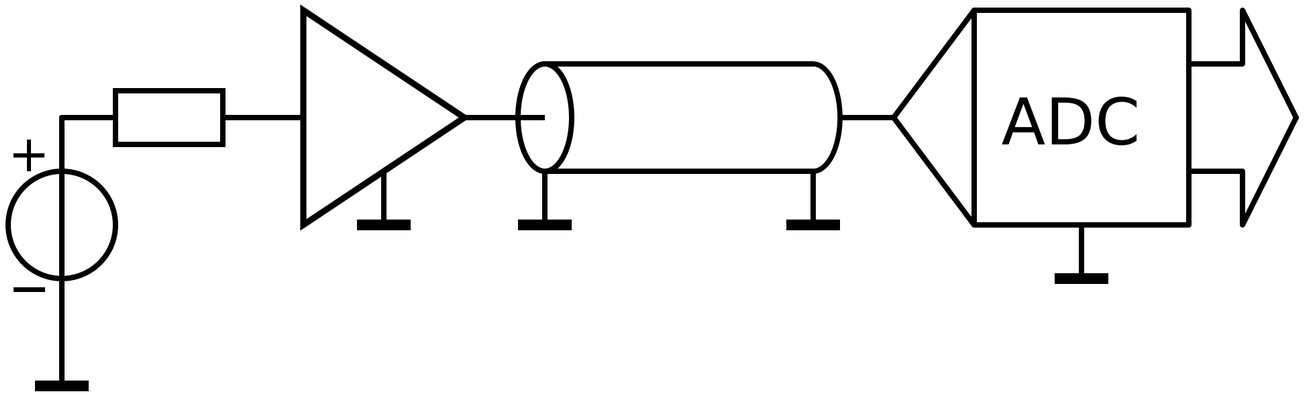


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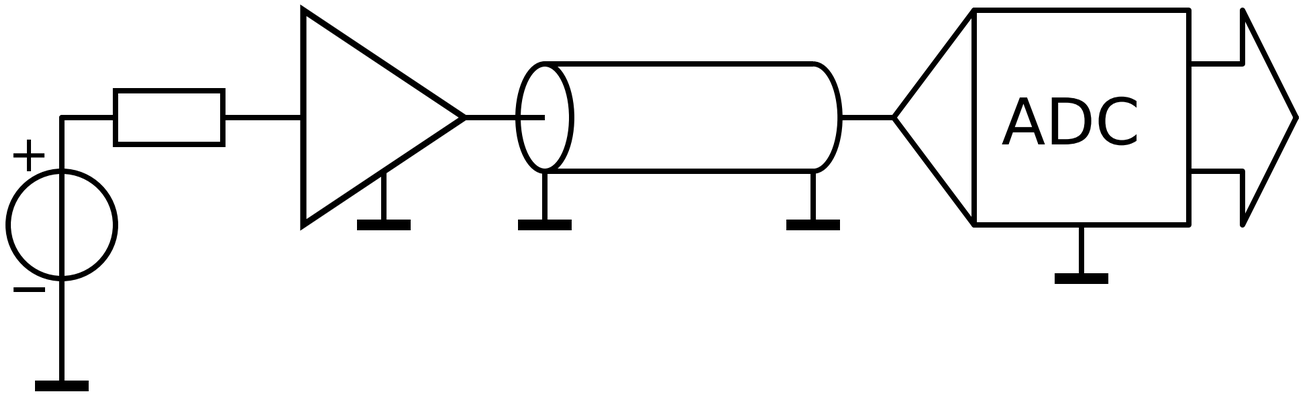


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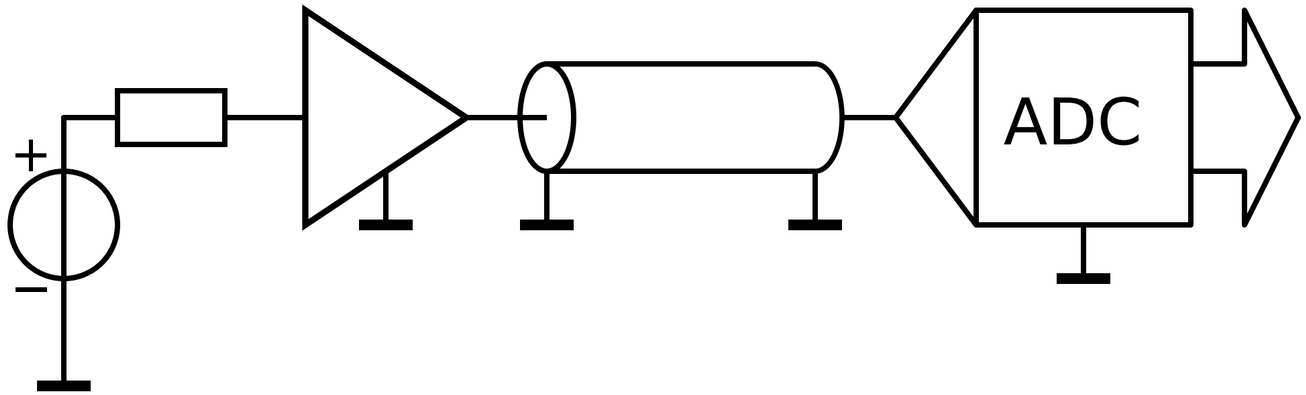


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Noise figure < 3dB

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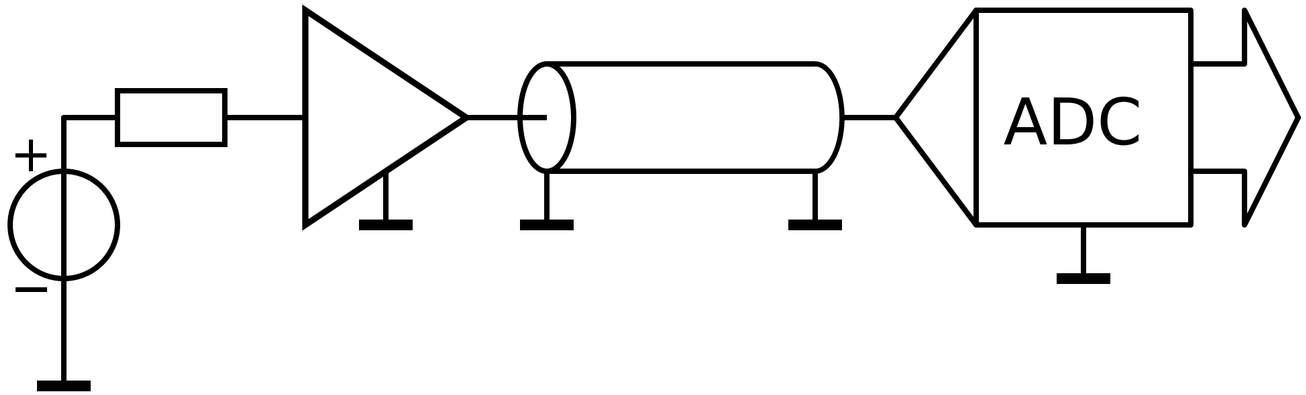


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Supply voltage: 5V

 

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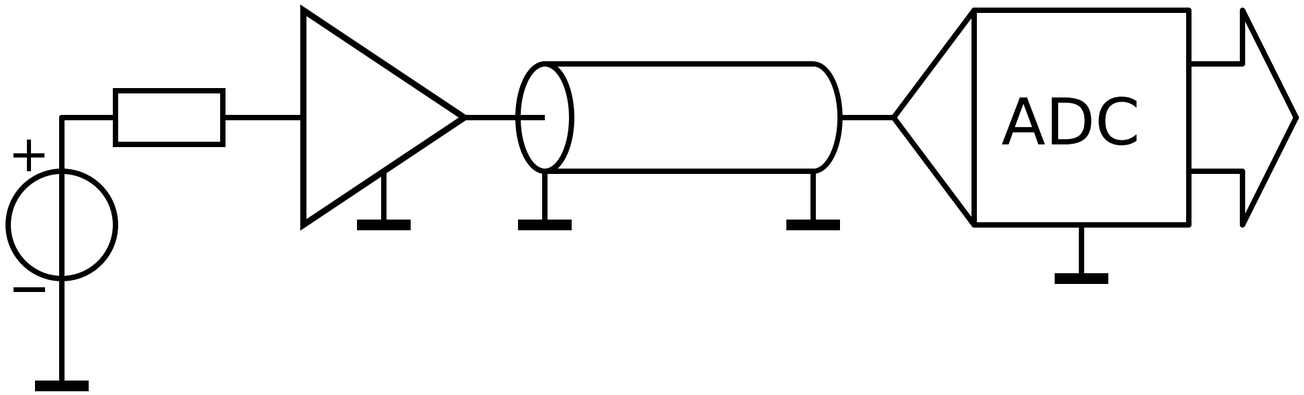


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Supply voltage: 5V

Operating temperature: room temperature

 

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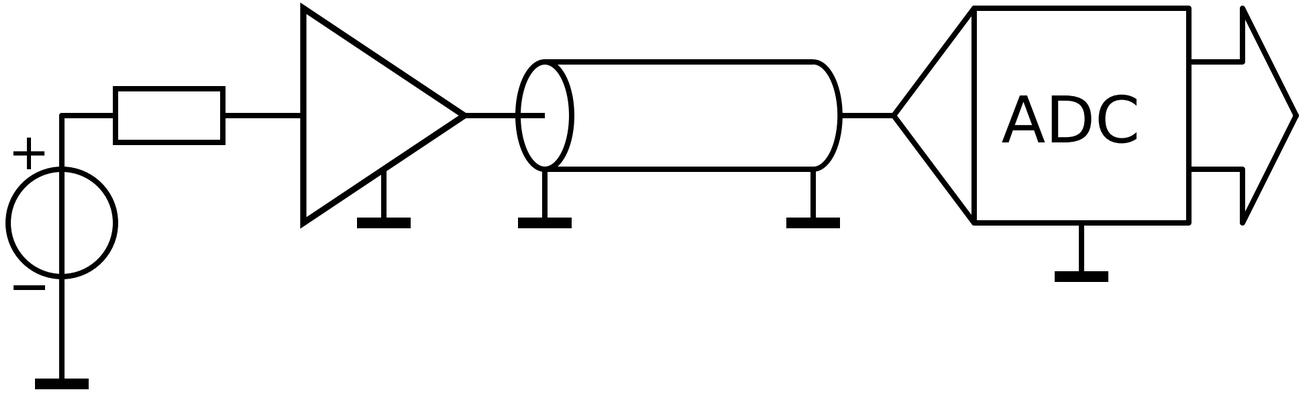


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## Amplifier performance requirements

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| | |
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| P1 Input impedance | >> 600 Ohm |
| P2 Input voltage | 50 $mV_{pp}$ |
| P3 Load capacitance | 3400 pF |
| P4 Quiescent load voltage | 2.5 $V_{DC}$ |
| P5 Load signal voltage | 4.5 $V_{pp}$ |
| P6 Rate of change output voltage | >=1.41 V/us |
| P7 Noise figure @ 600 Ohm | <= 3 dB |
| P8 Small-signal bandwidth | 100Hz ... 500kHz |
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| | |
|---|---|
| E1 Operating temperature | 20 deg. Celsius |

# Design of amplifier configuration

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Voltage transfer independent of
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$$A_v = \frac{V_\ell}{V_s} = \frac{4.5}{0.05} = 90$$

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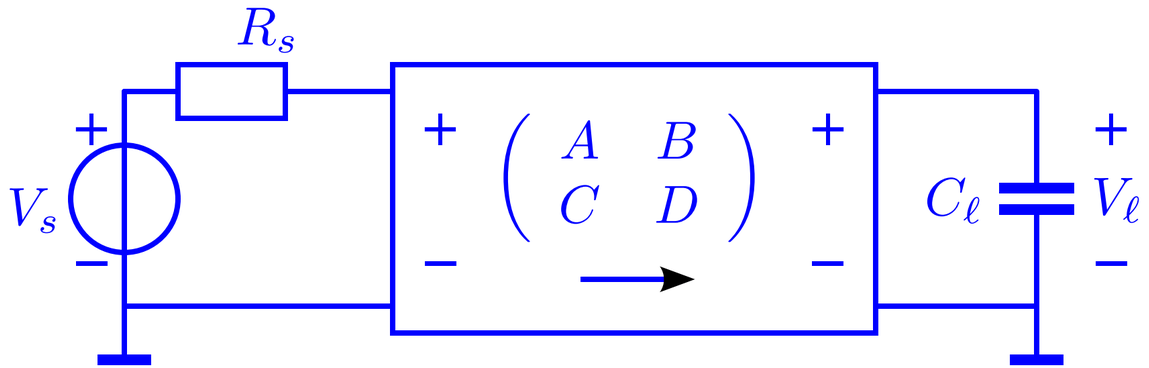


$$A = \frac{1}{A_v},\ B = 0,\ C = 0,\ D = 0$$

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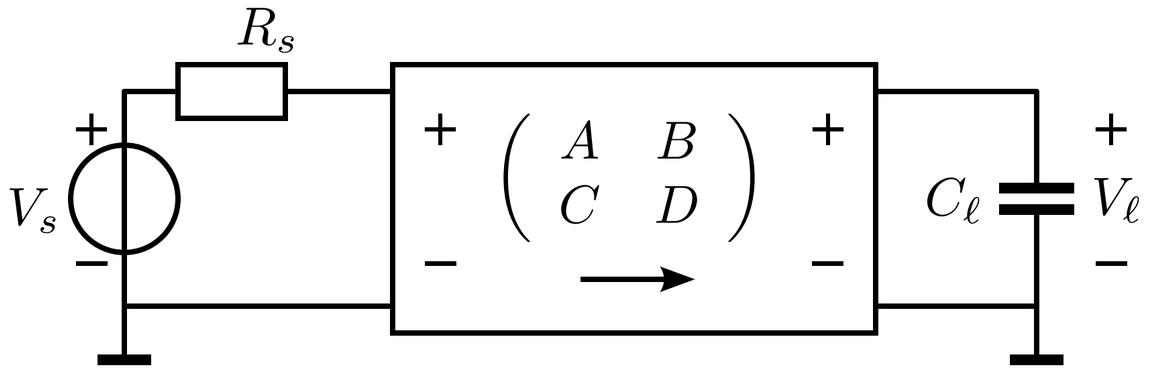


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Amplifier concept for establishing a nonzero value for A only

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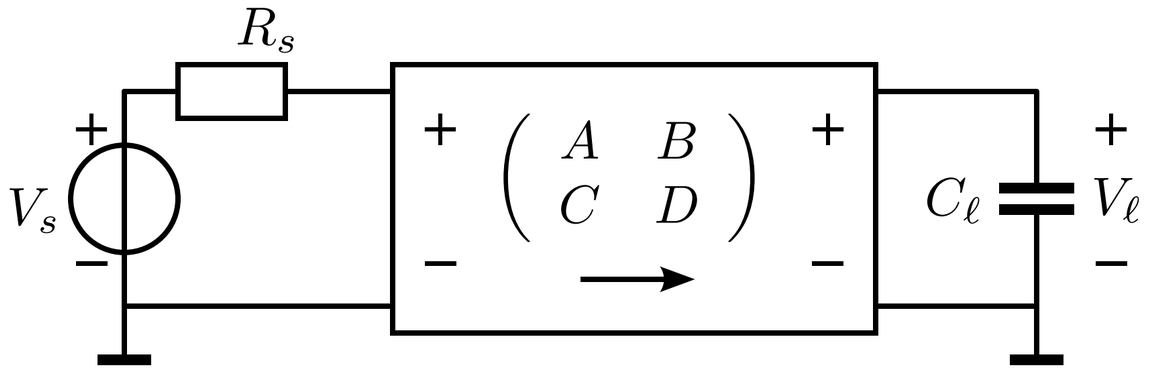


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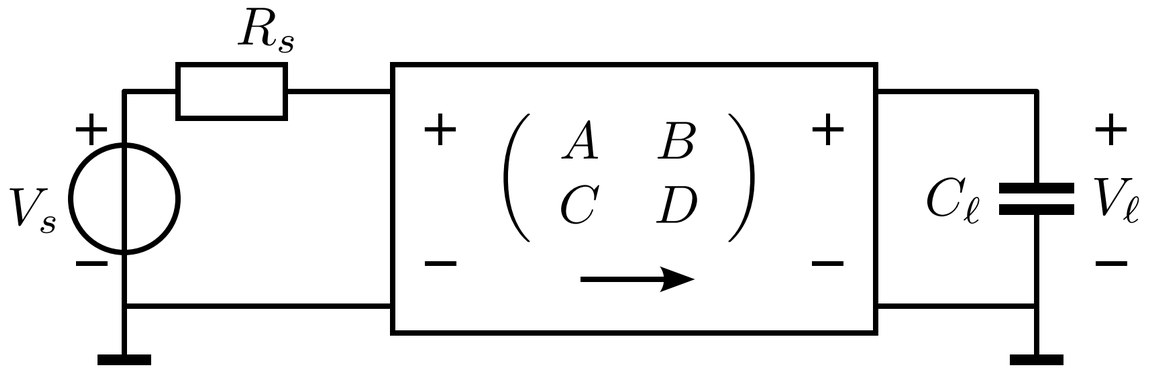


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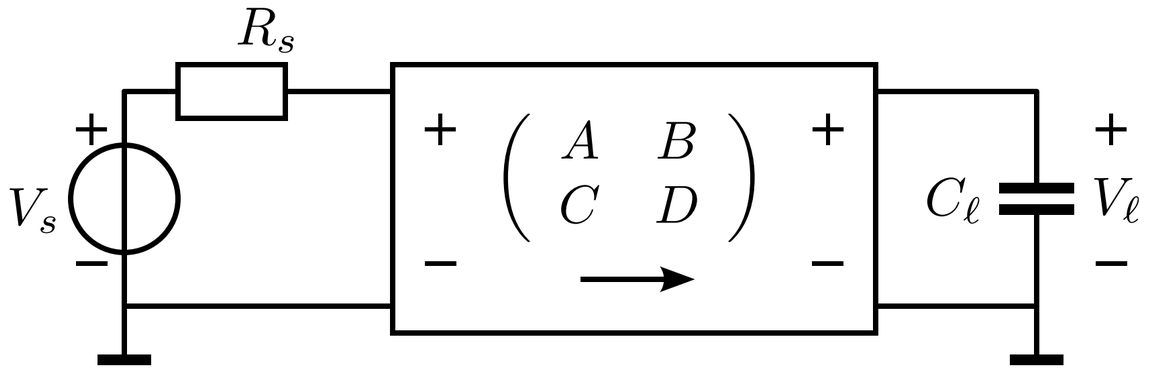


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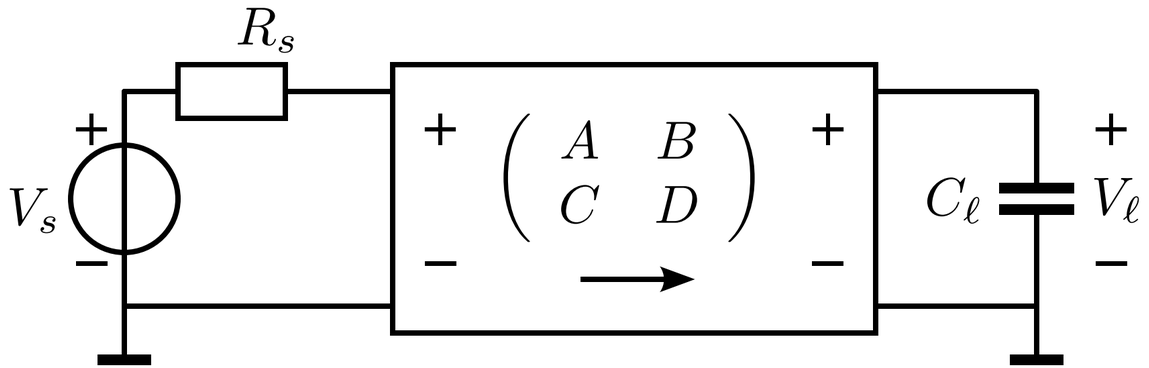


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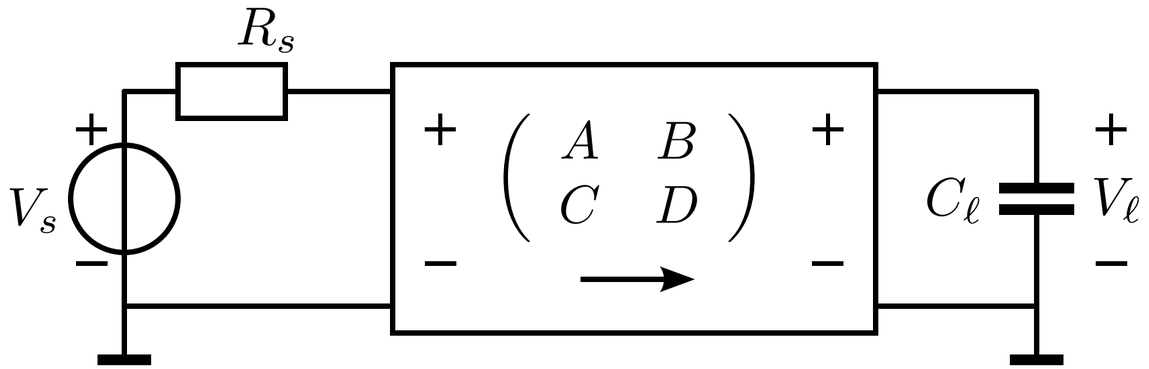


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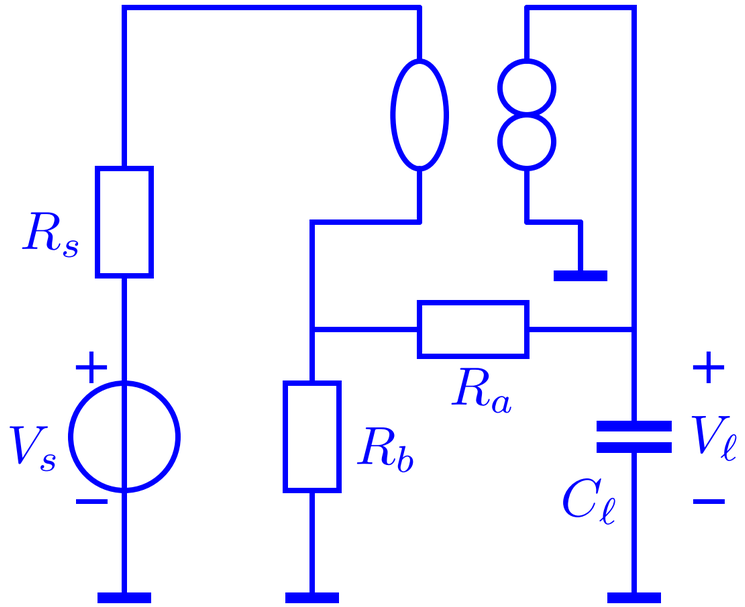

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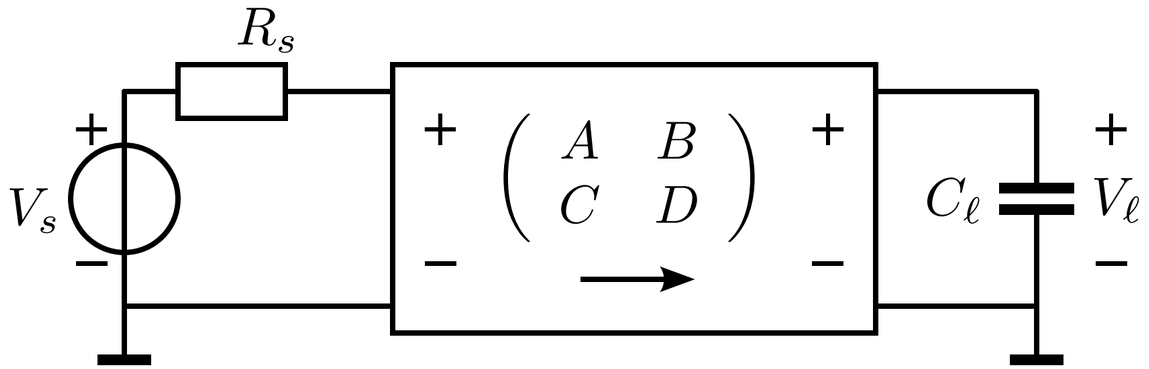


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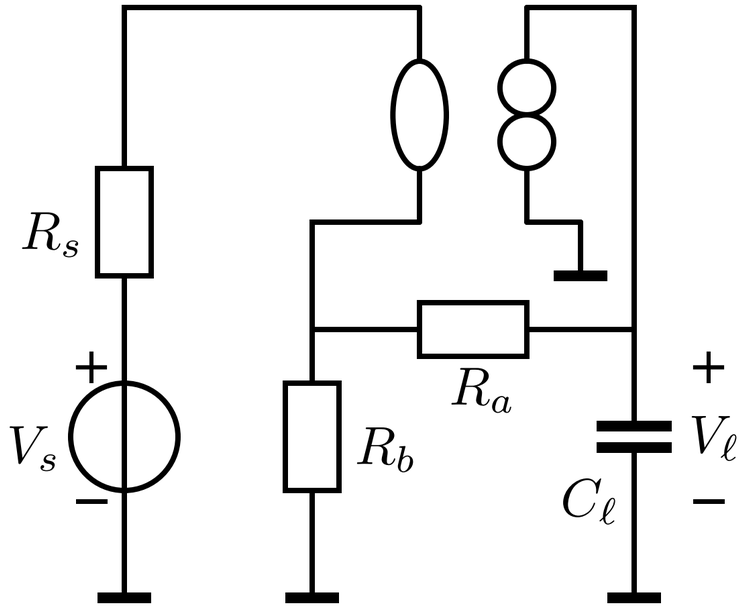


Nonzero value for A:

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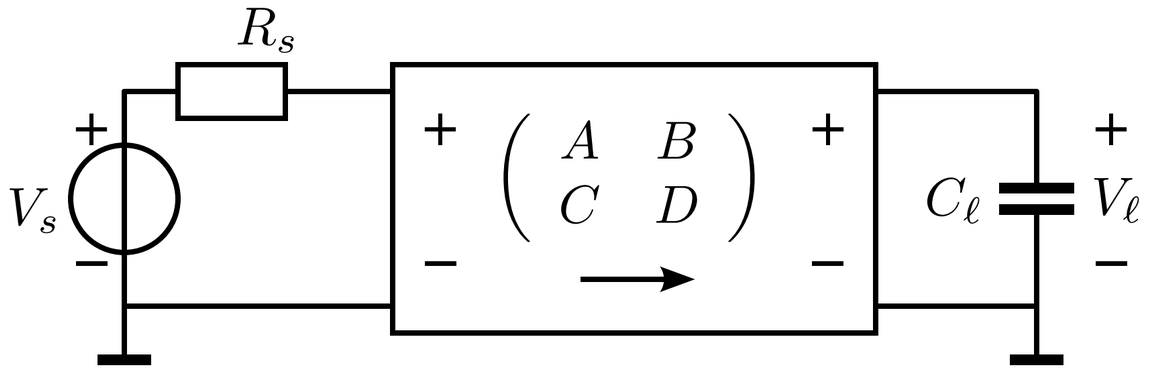


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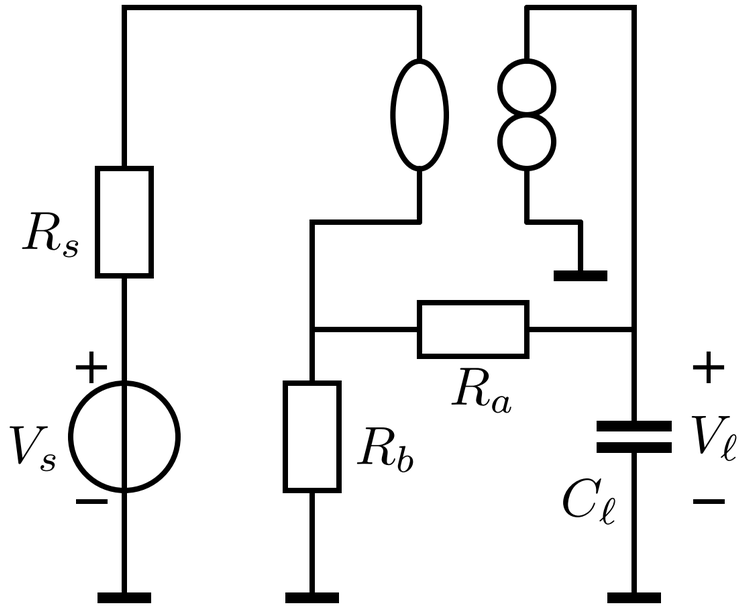


Nonzero value for A:

Parallel sensing

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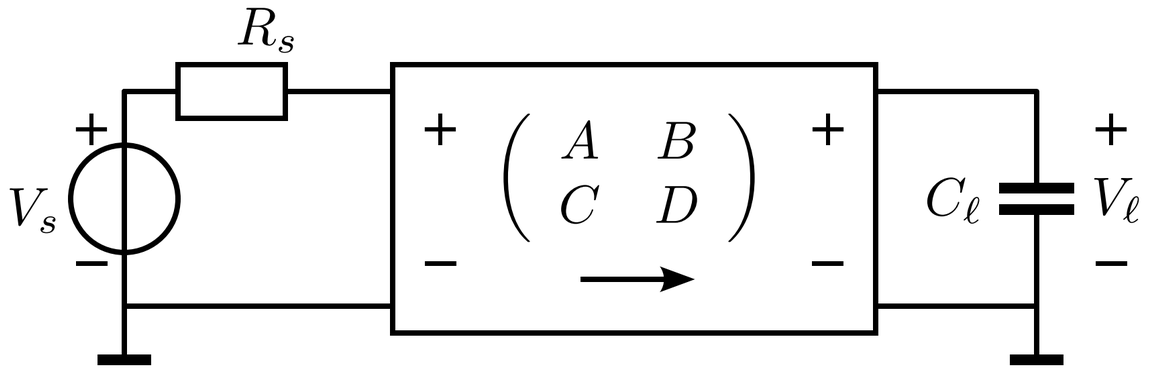


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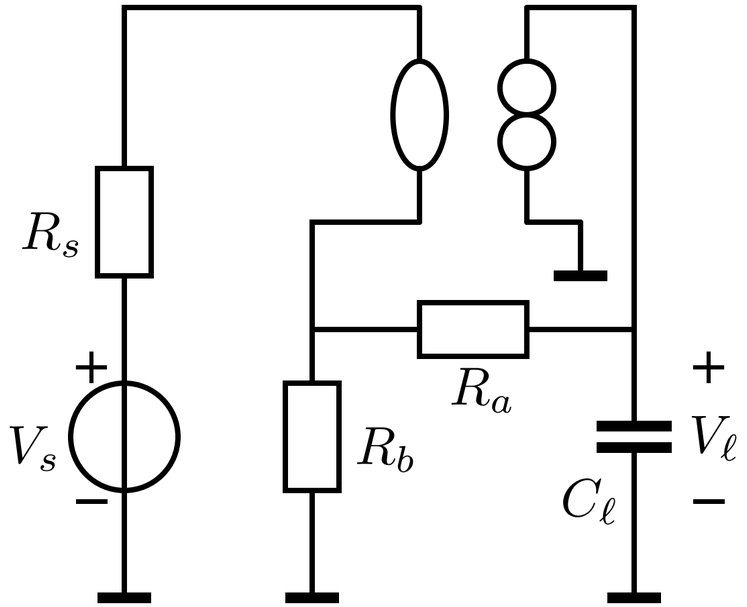
Passive feedback configuration

- Feedback network increases noise and power losses of controller




Nonzero value for A:

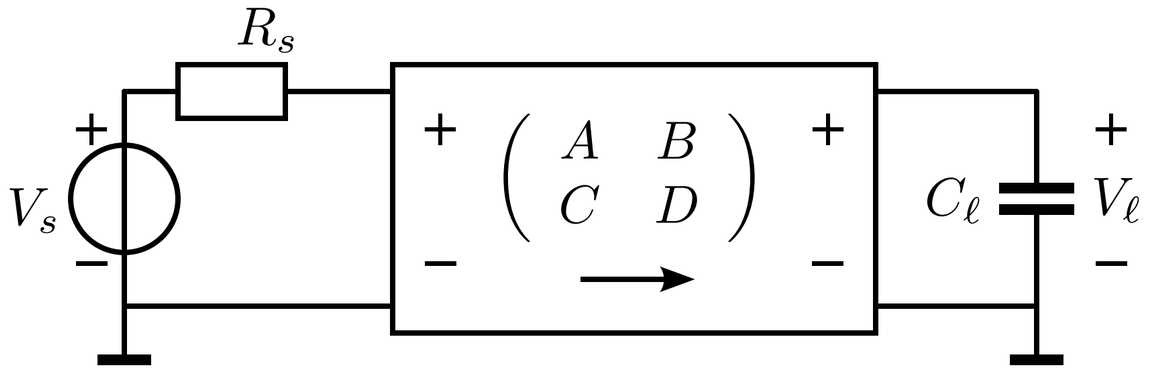
Parallel sensing

Zero output impedance

# Design of amplifier configuration

Voltage transfer independent of source and load impedance.

$$A_v = \frac{V_\ell}{V_s} = \frac{4.5}{0.05} = 90$$




$$A = \frac{1}{A_v},\ B = 0,\ C = 0,\ D = 0$$

Amplifier concept for establishing a nonzero value for A only

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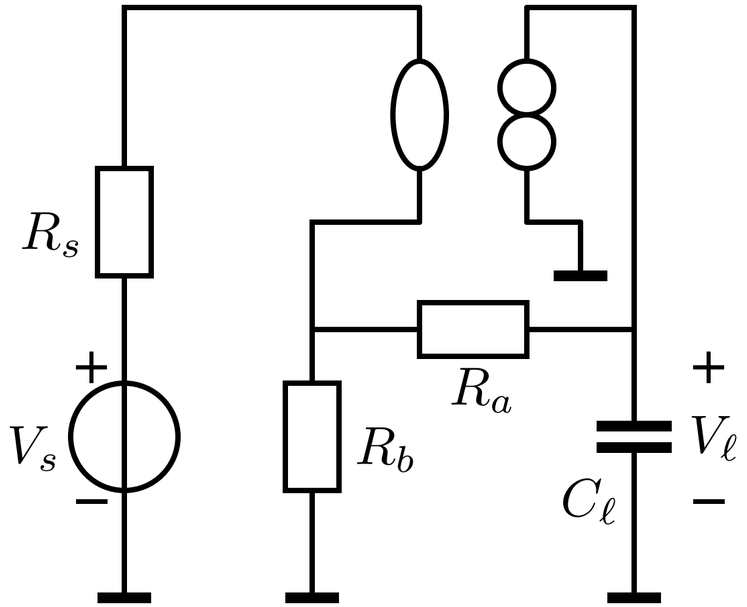


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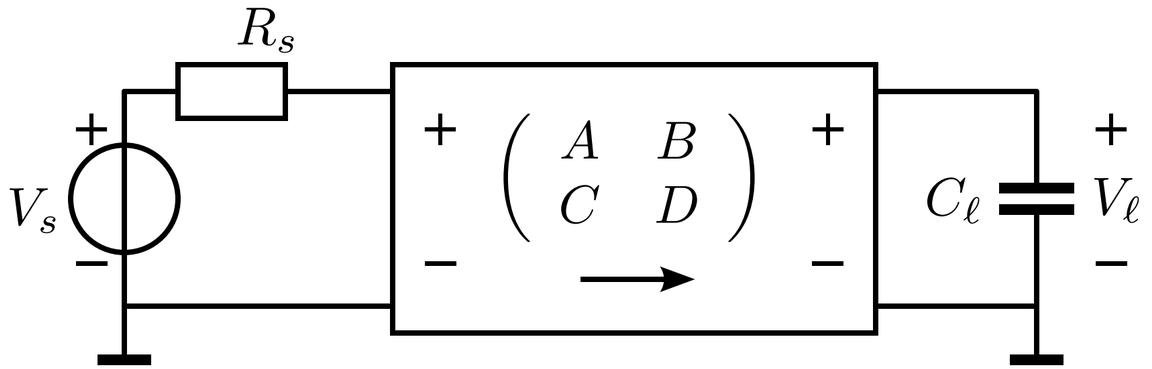


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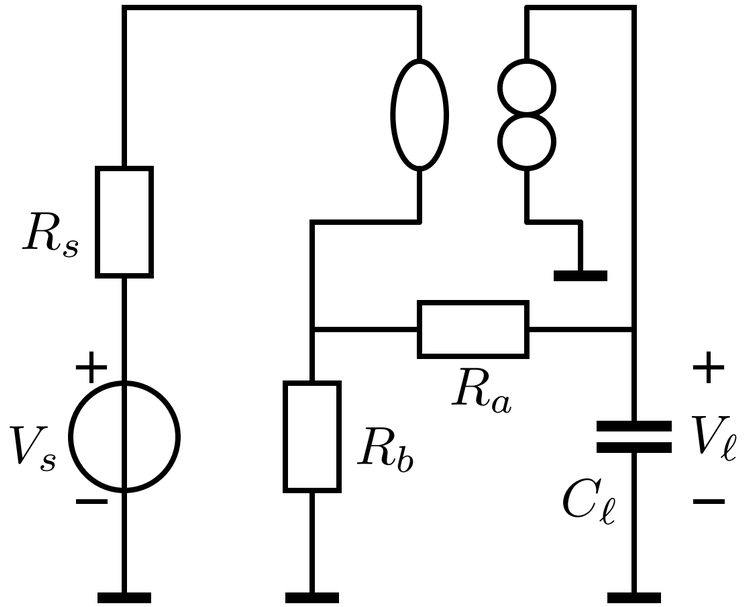


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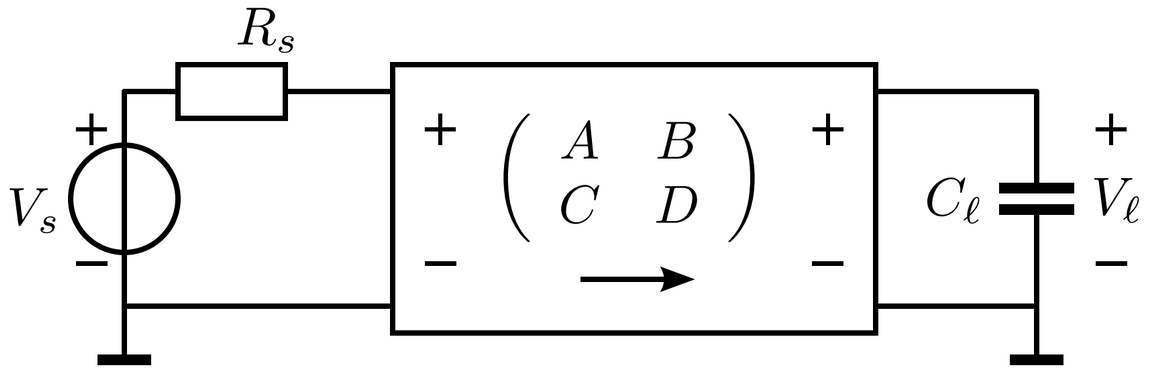


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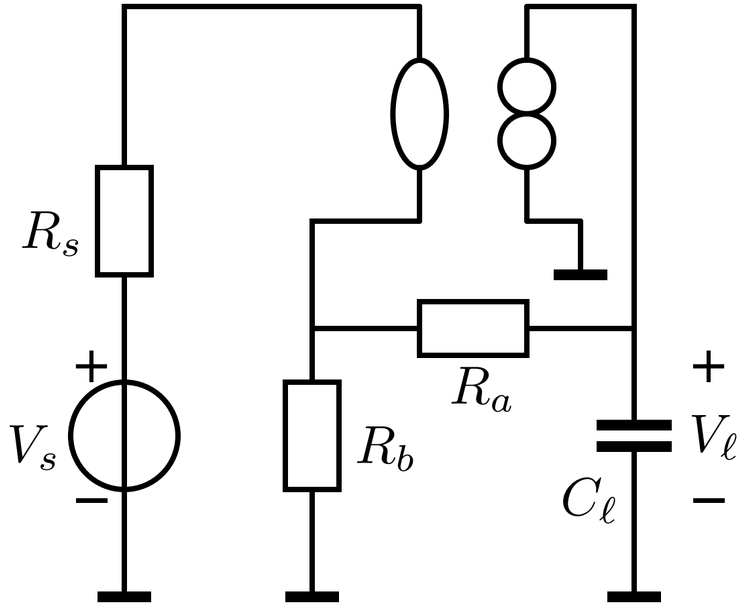


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# Noise design

# Noise design

Find and solve design equations for elements that contribute to the noise

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1. Feedback resistors

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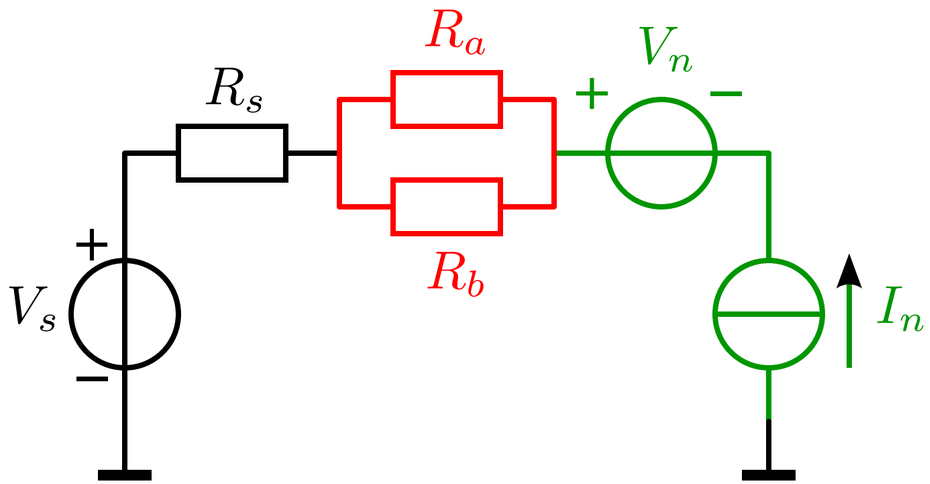

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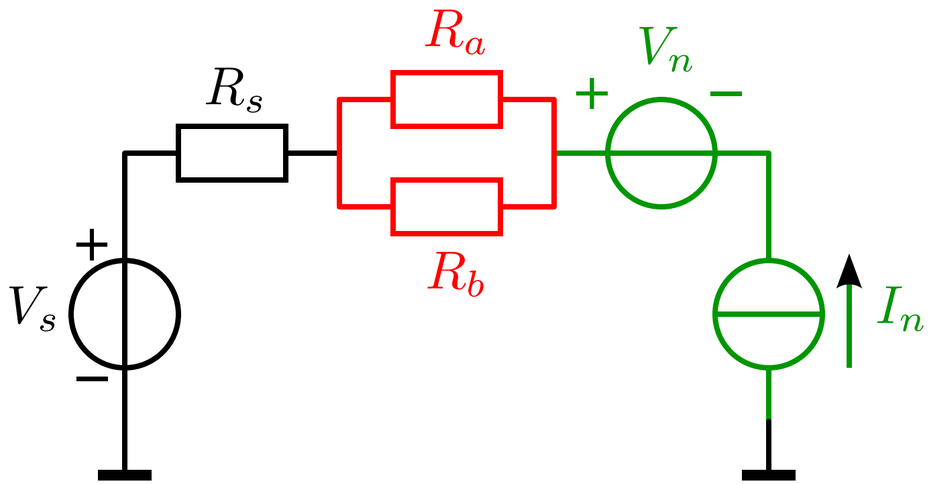


$$S_{v_{tot}} = 4kT\left(R_s + R_a||R_b\right) + S_{V_n} + S_{I_n}\left(R_s + R_a||R_b\right)^2$$

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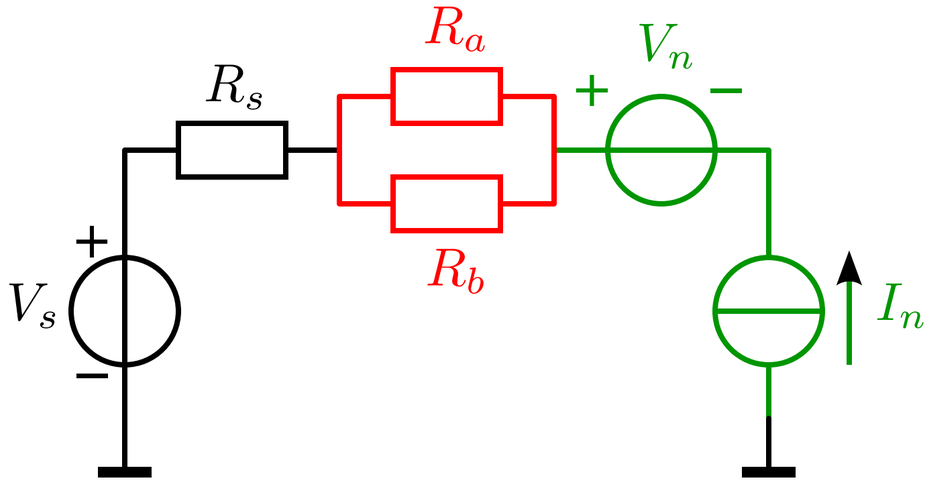


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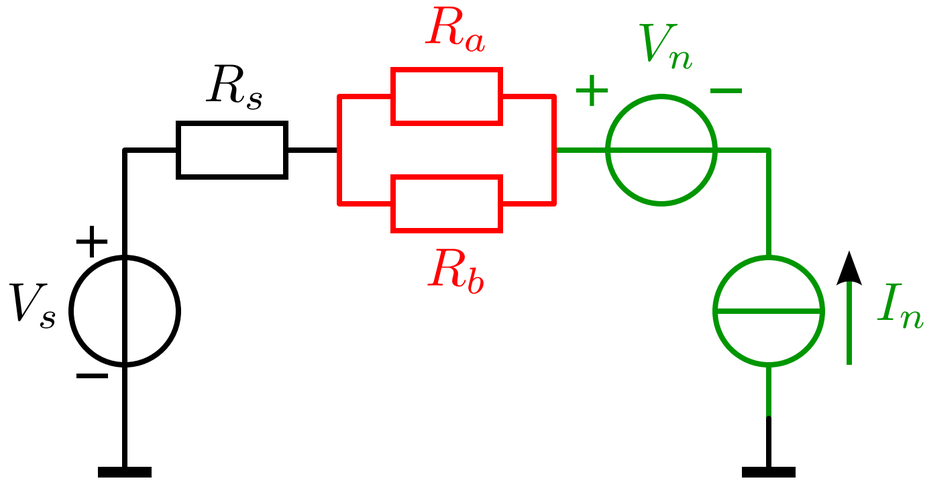


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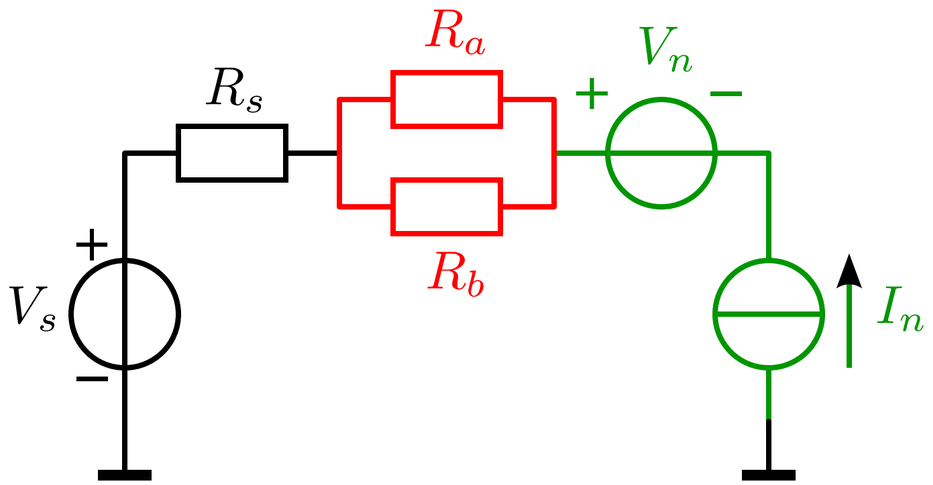


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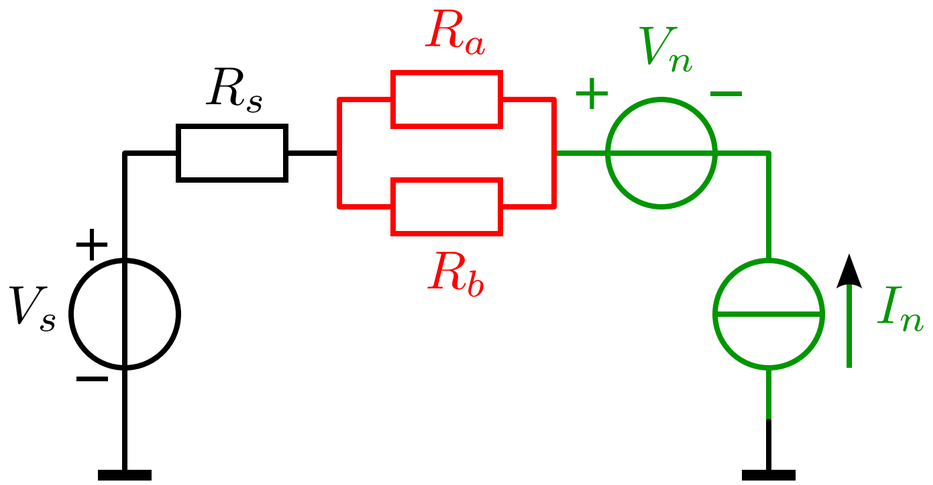


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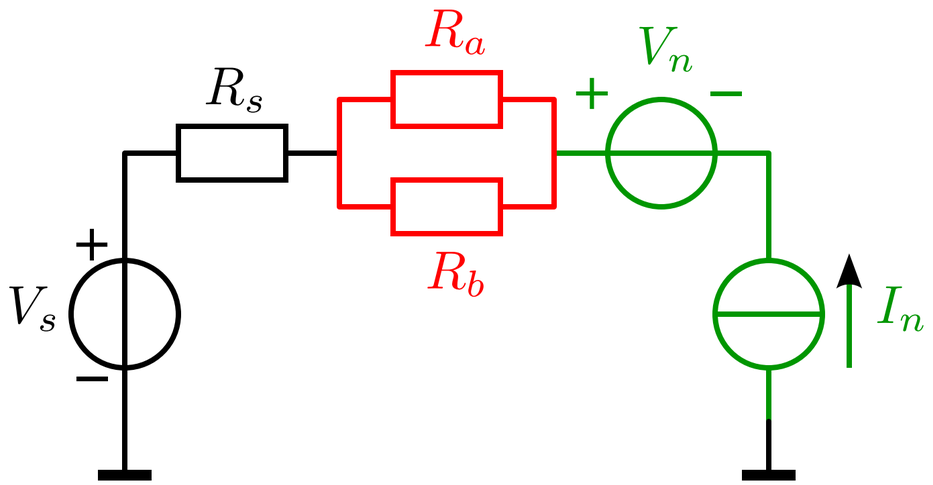


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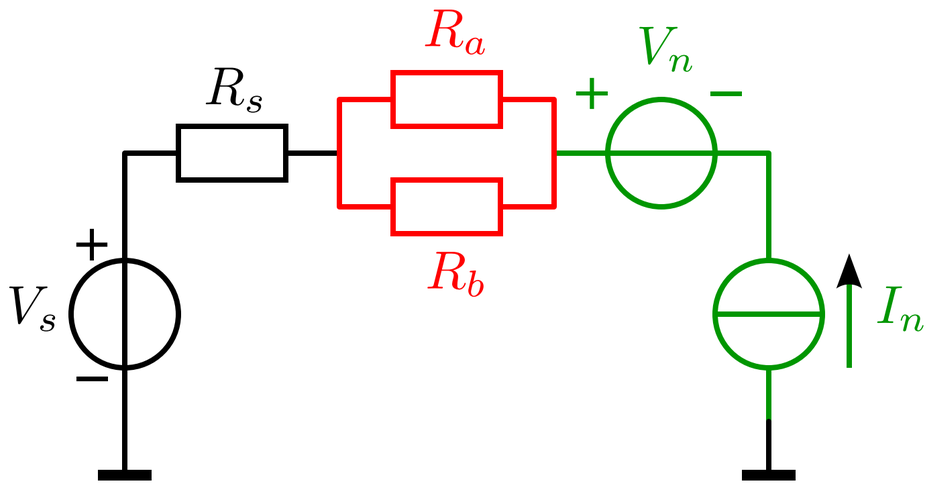


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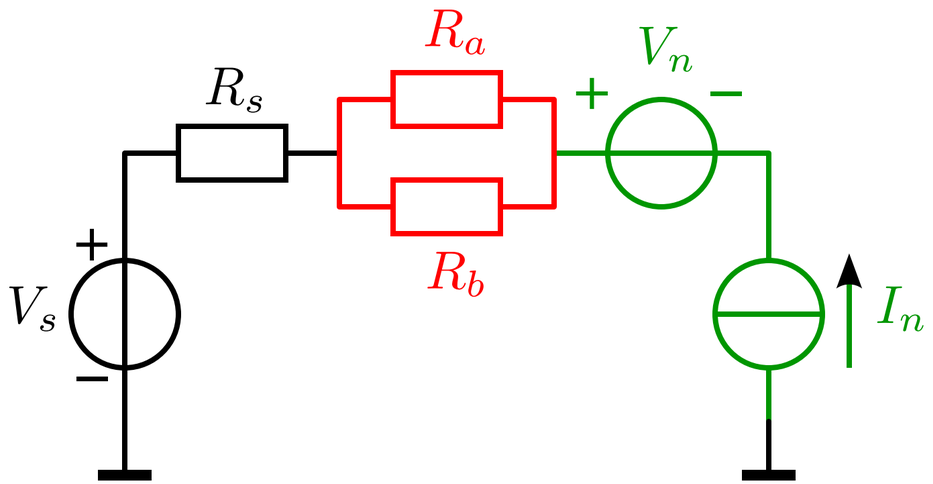


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No power consumption requirements

 

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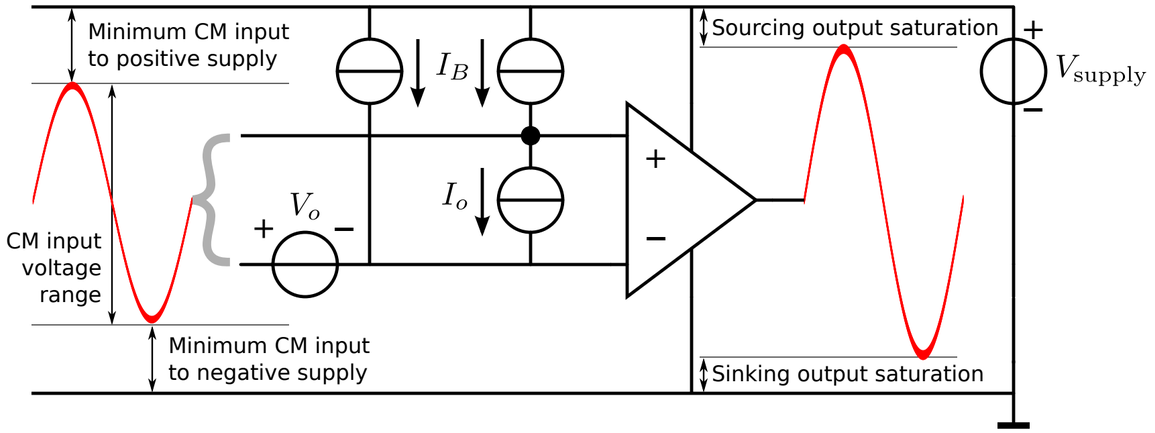

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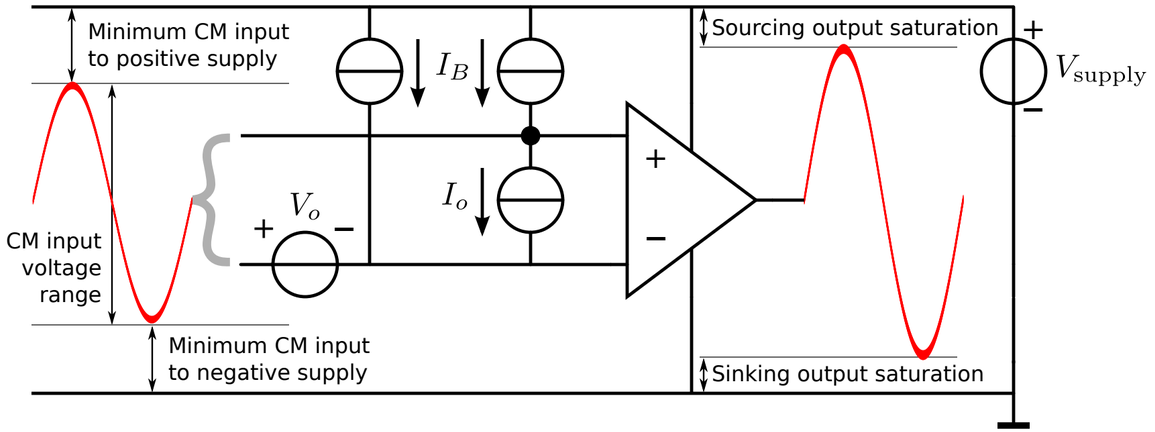

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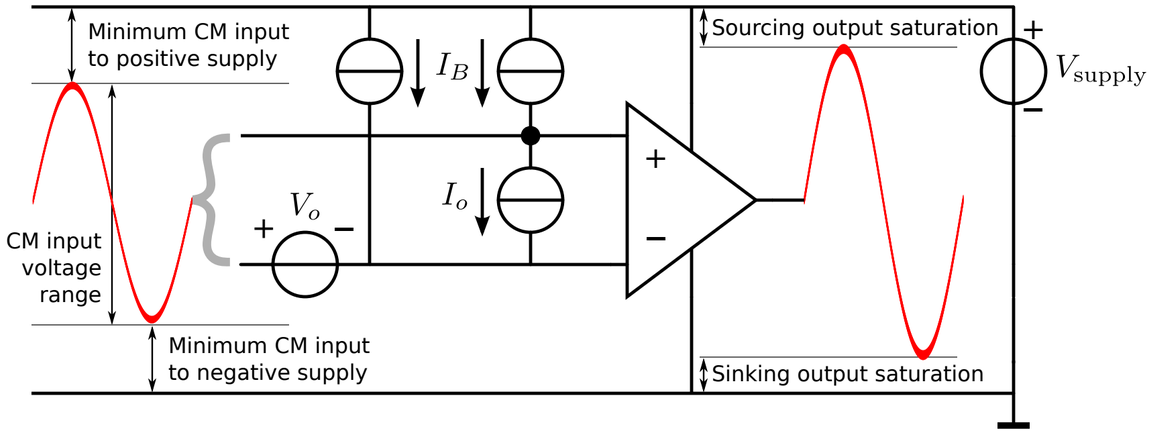


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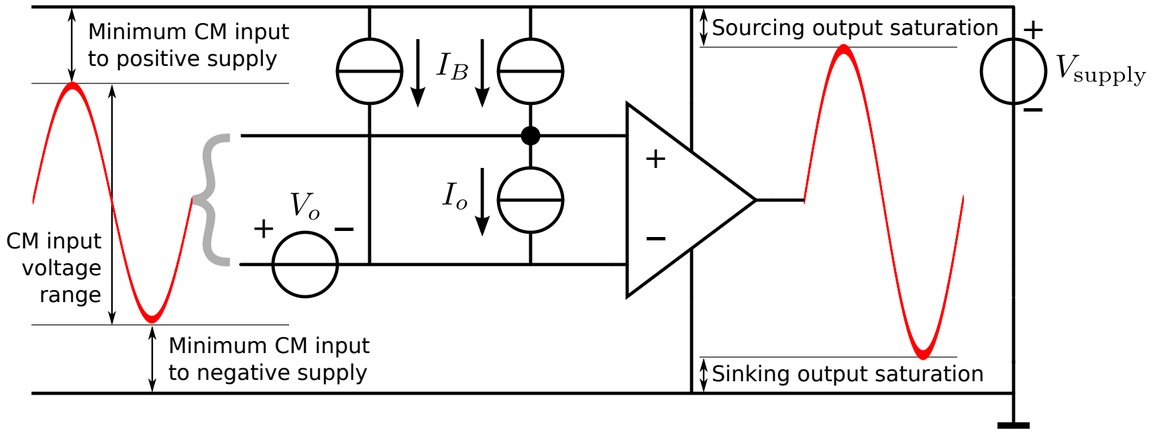


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Output saturation source/sink: < 0.25V - total output biasing error voltage

 

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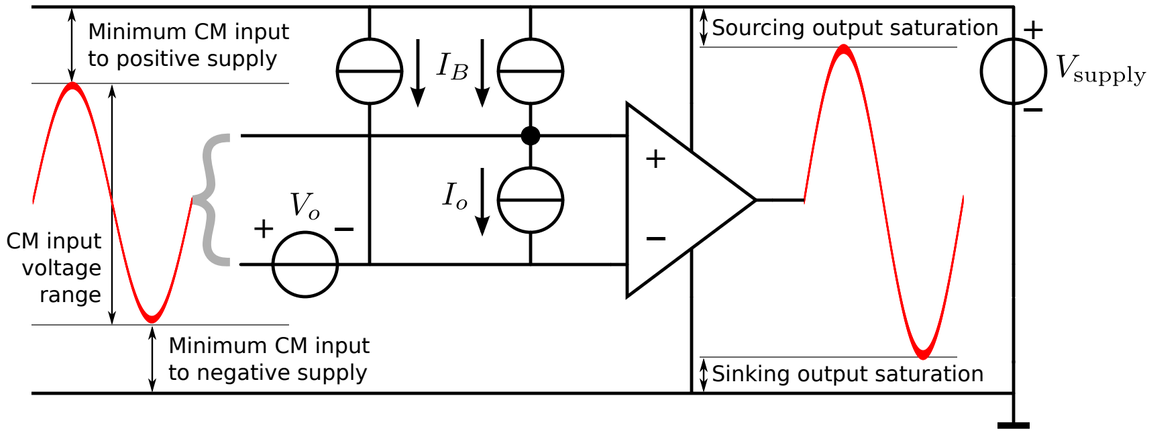


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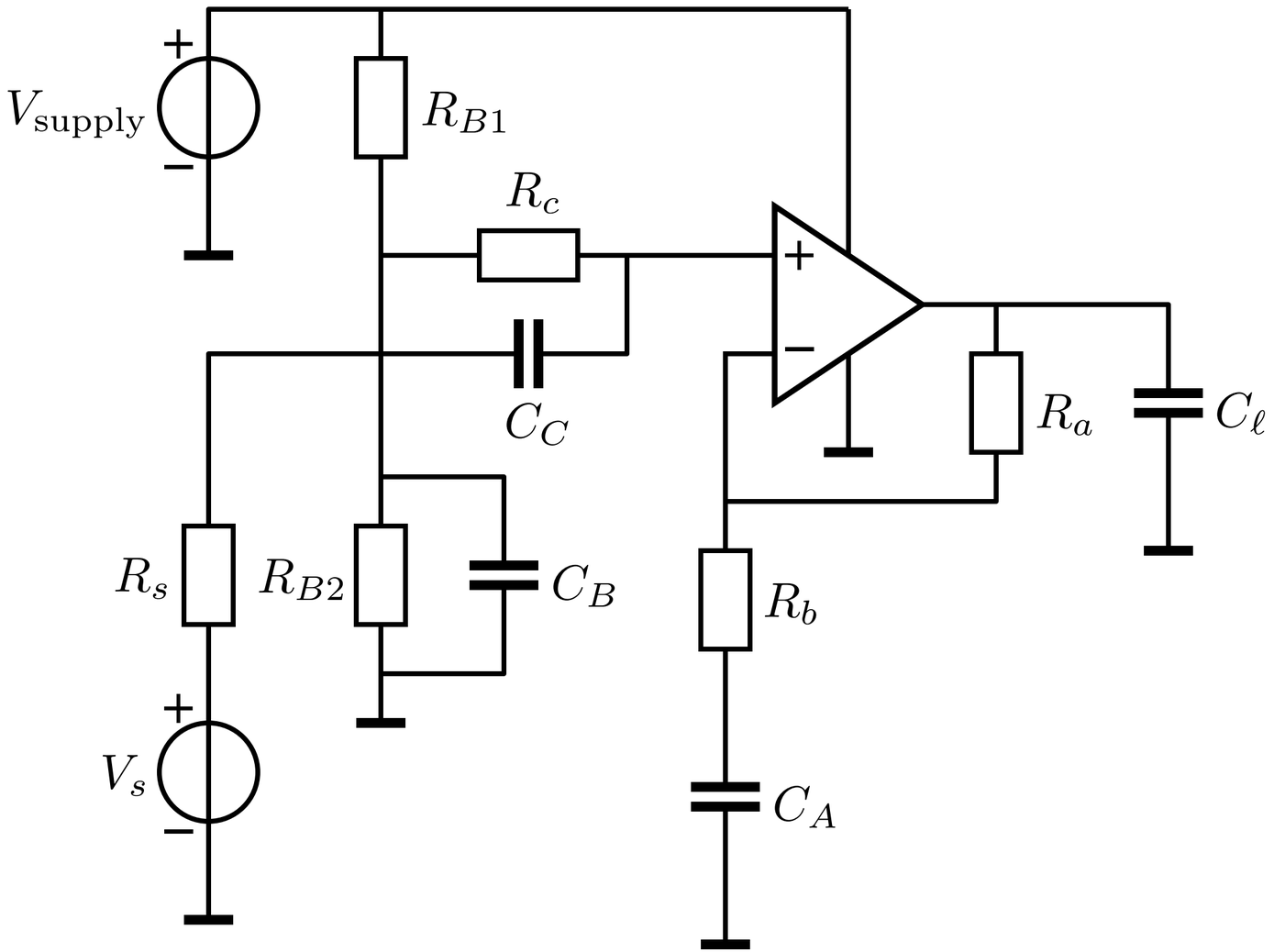

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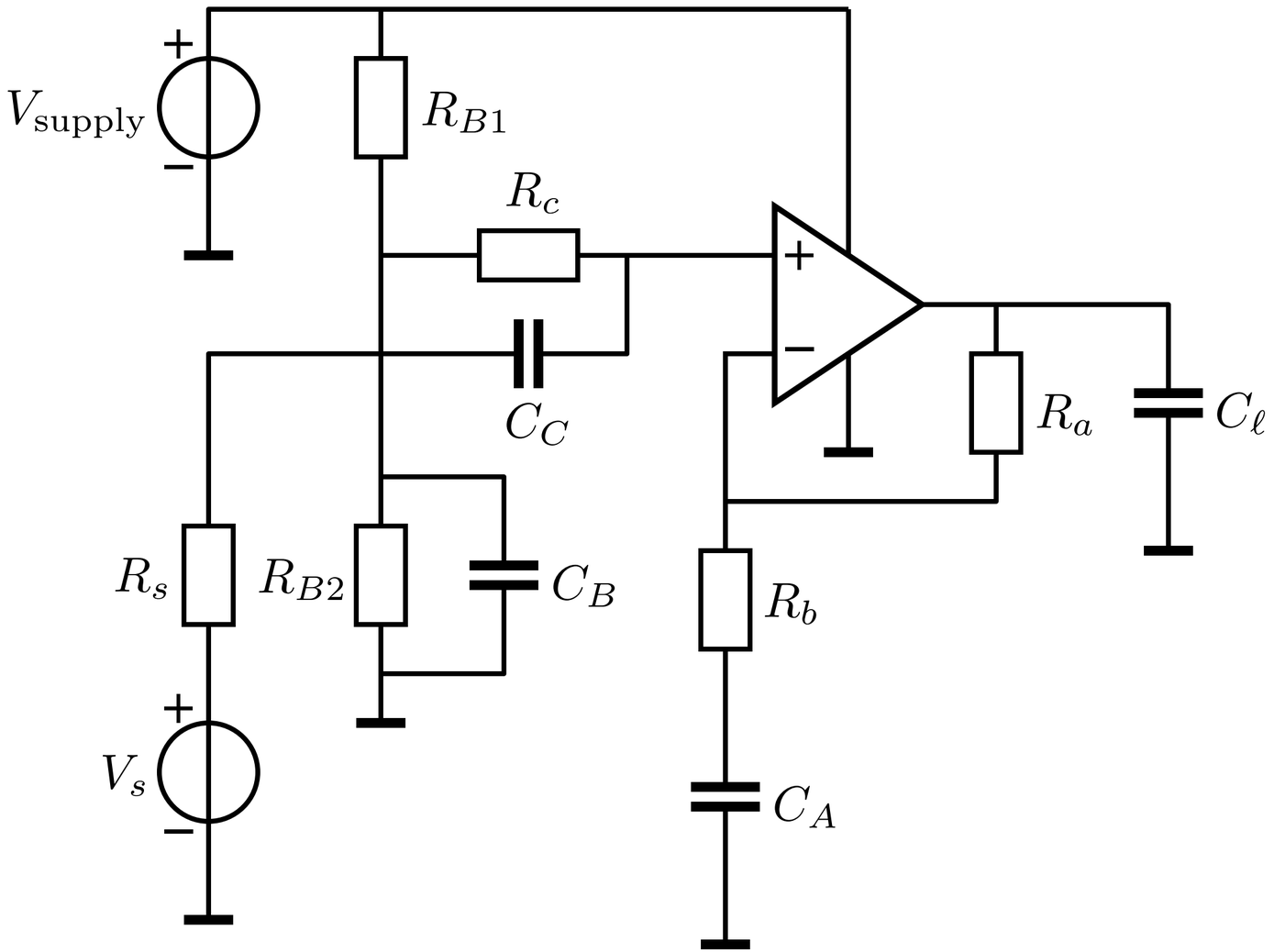


Contributions to biasing errors:

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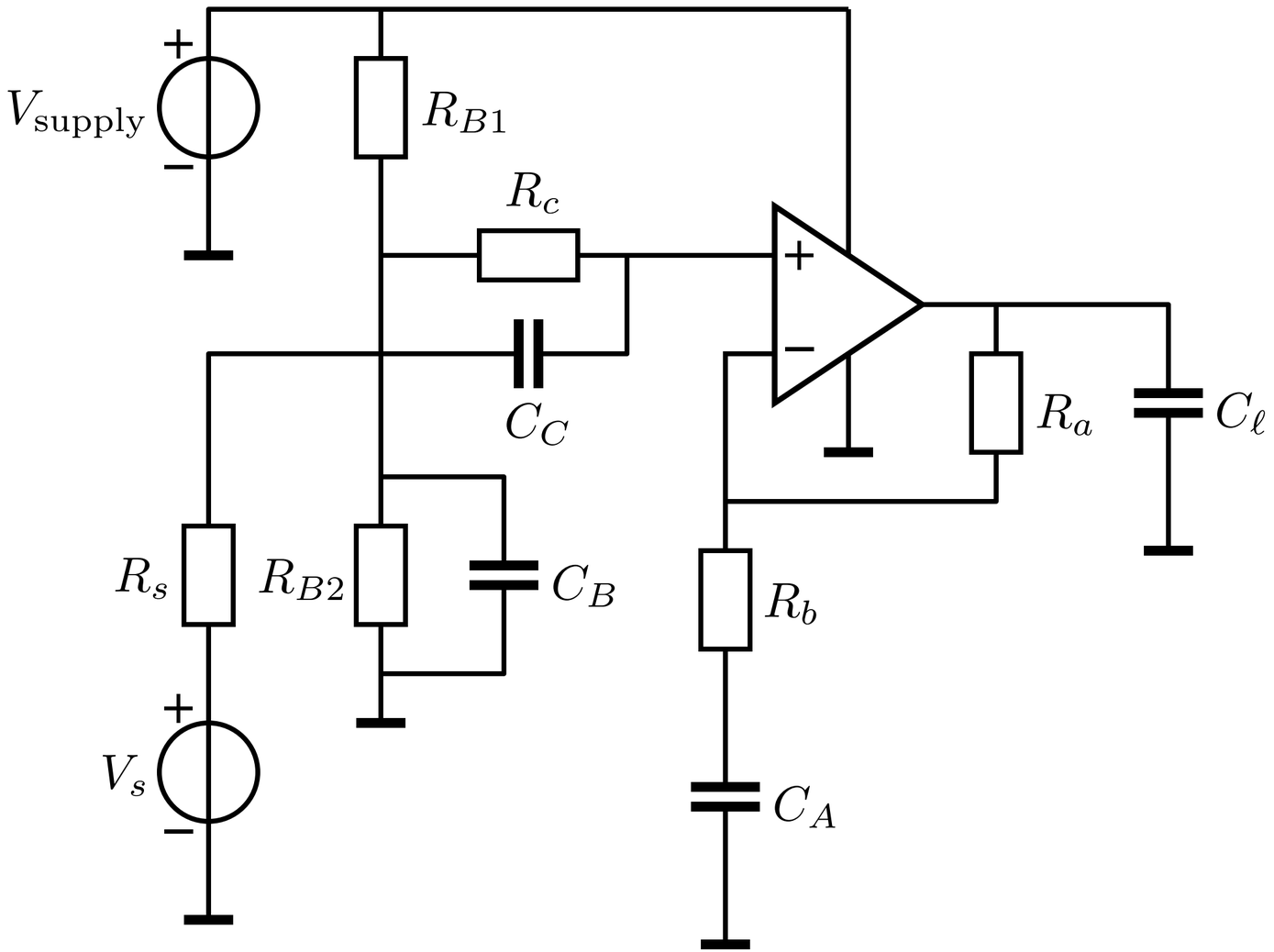


Contributions to biasing errors:

- Supply voltage tolerance

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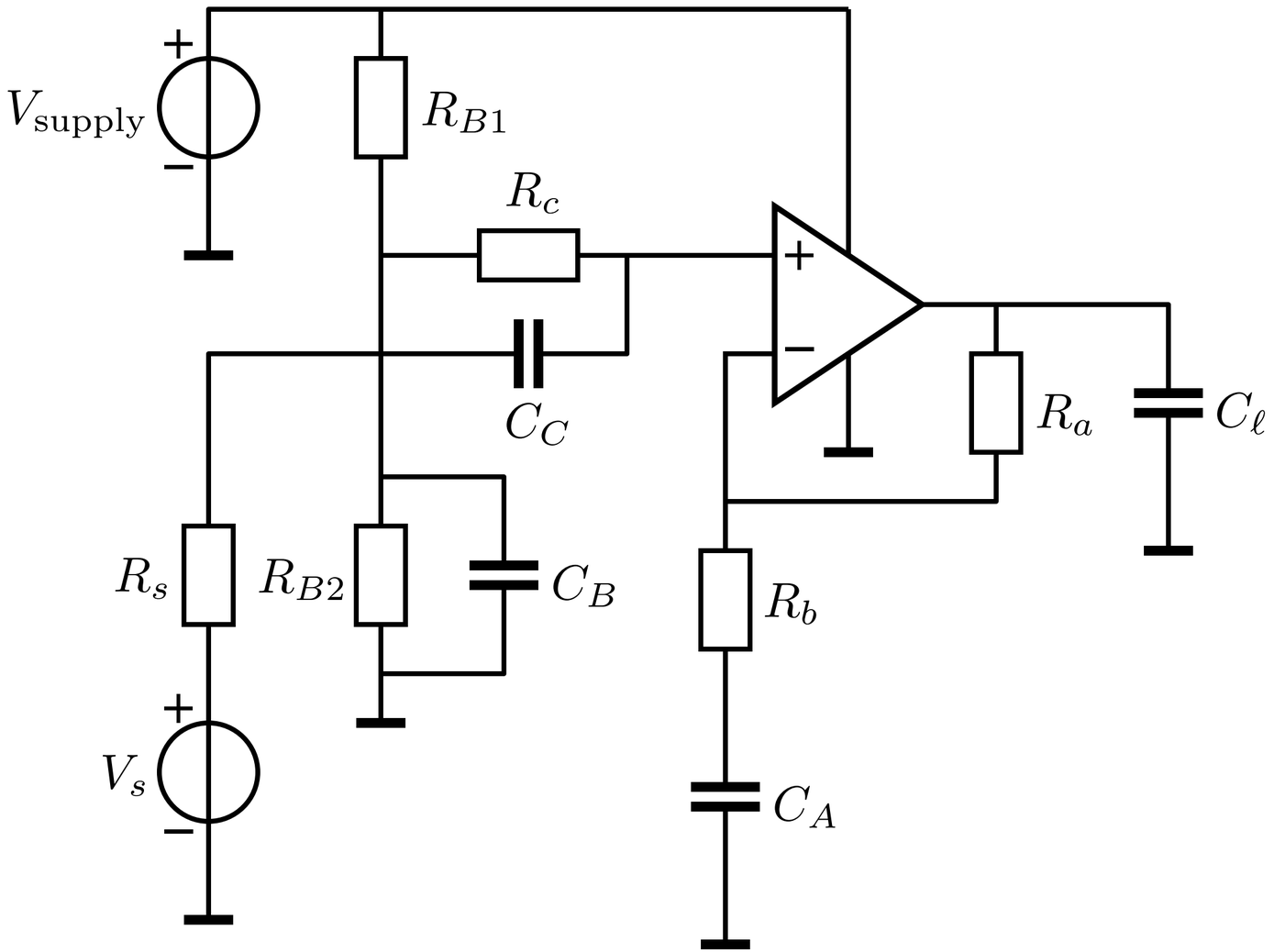


Contributions to biasing errors:

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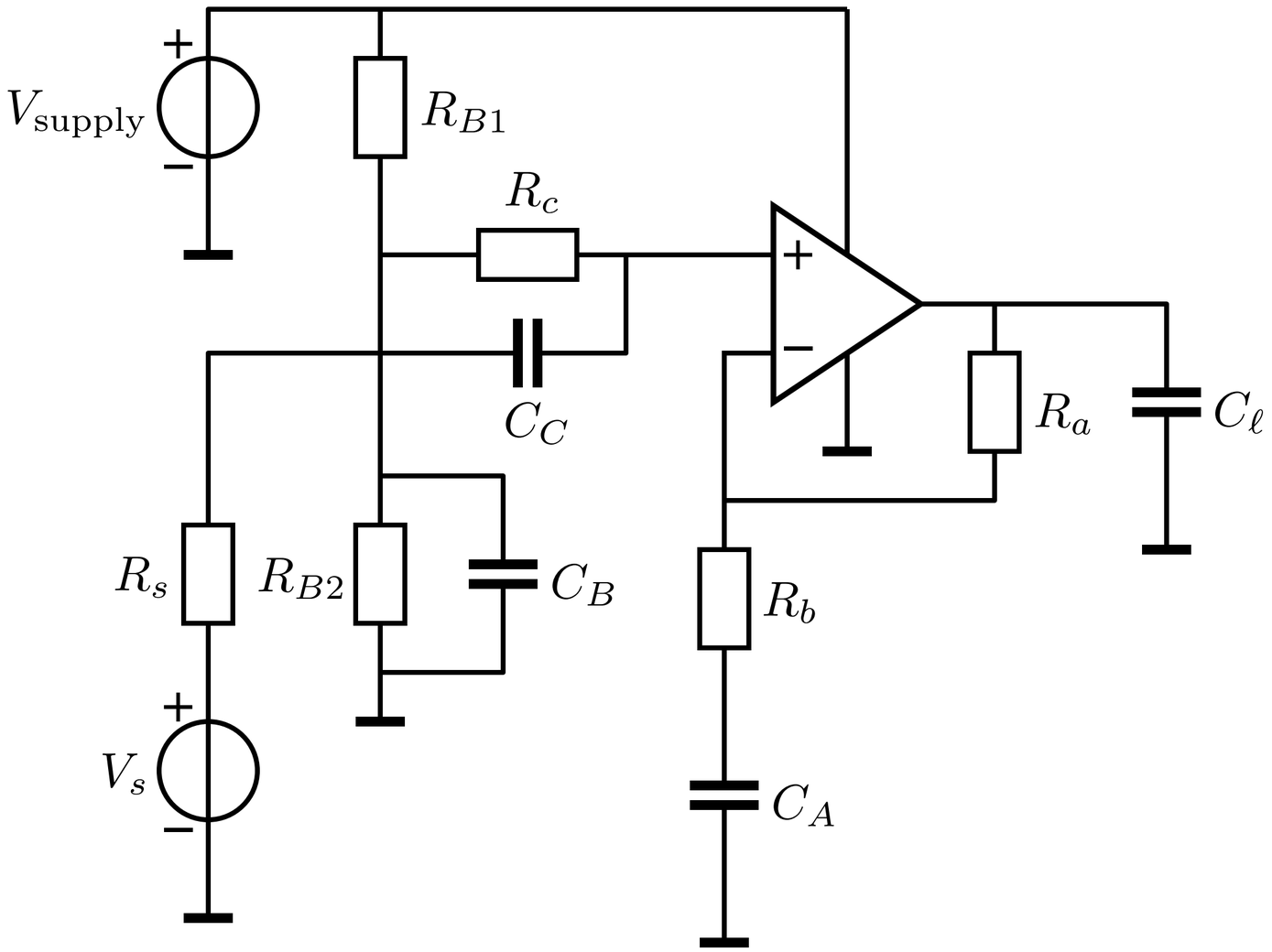
- Resistor tolerances

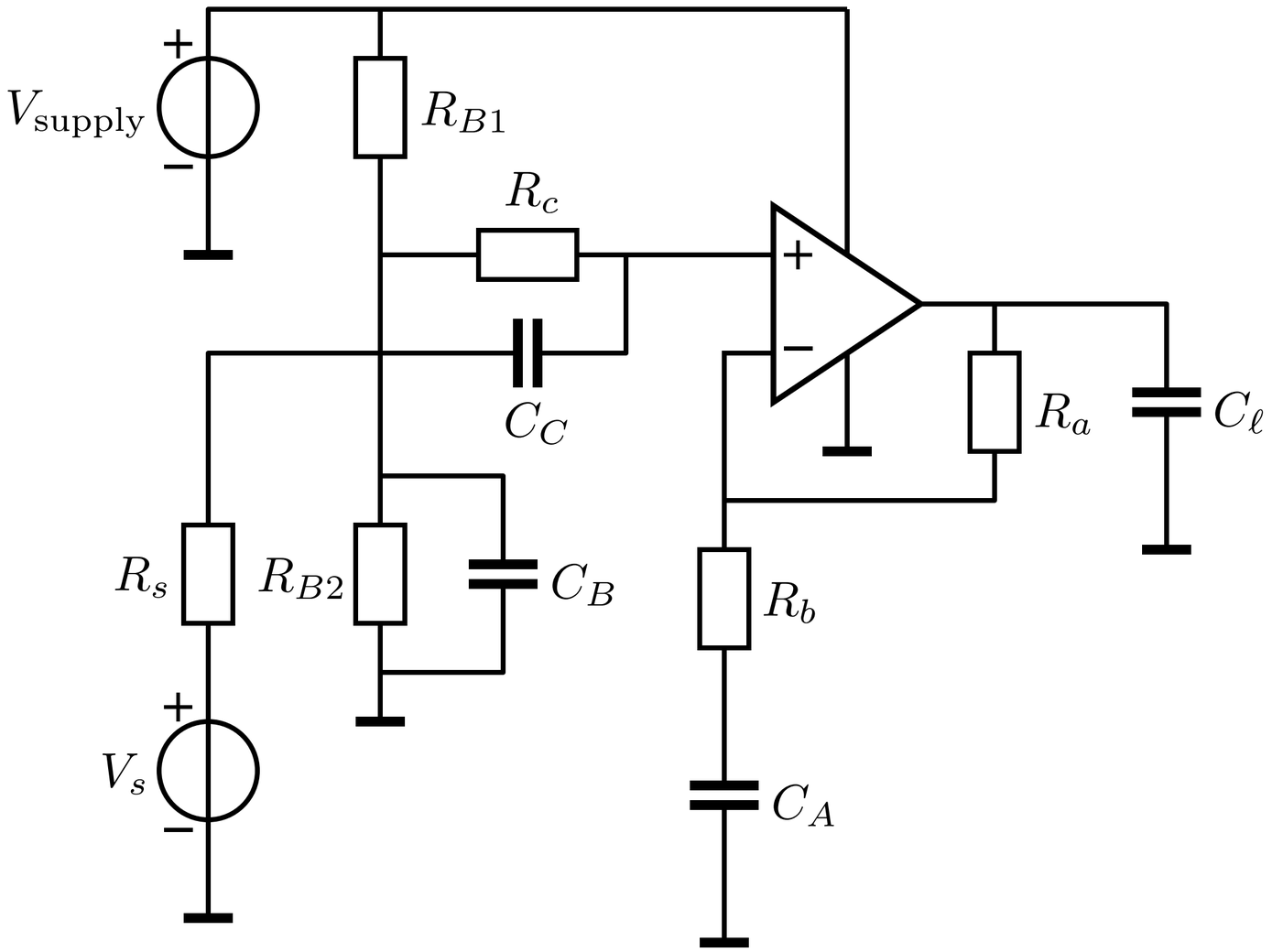
# Biasing errors




Contributions to biasing errors:

- Supply voltage tolerance
- Resistor tolerances
- Bias current OpAmp

# Biasing errors




Contributions to biasing errors:

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- Resistor tolerances
- Bias current OpAmp
- Offset current OpAmp

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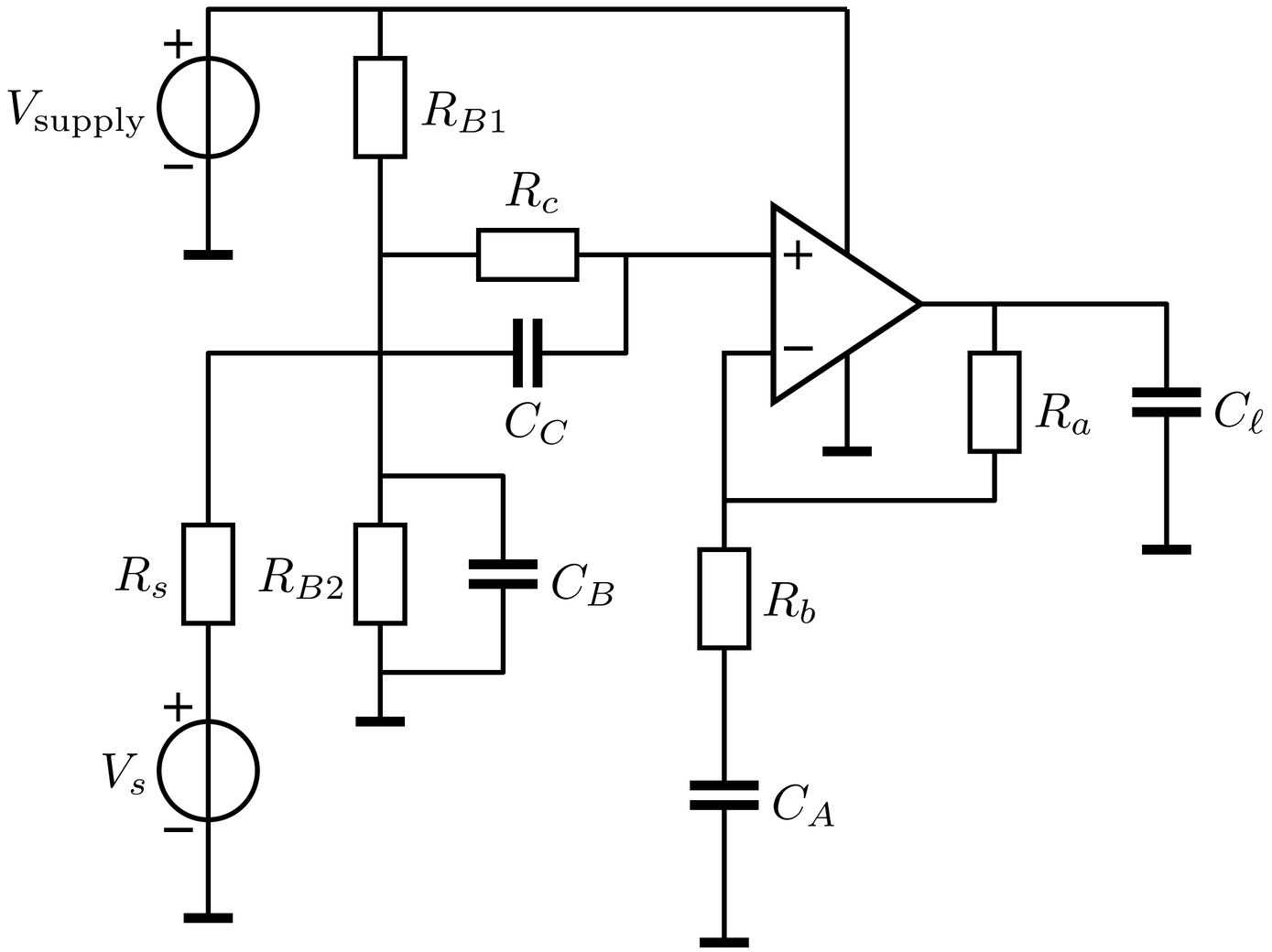


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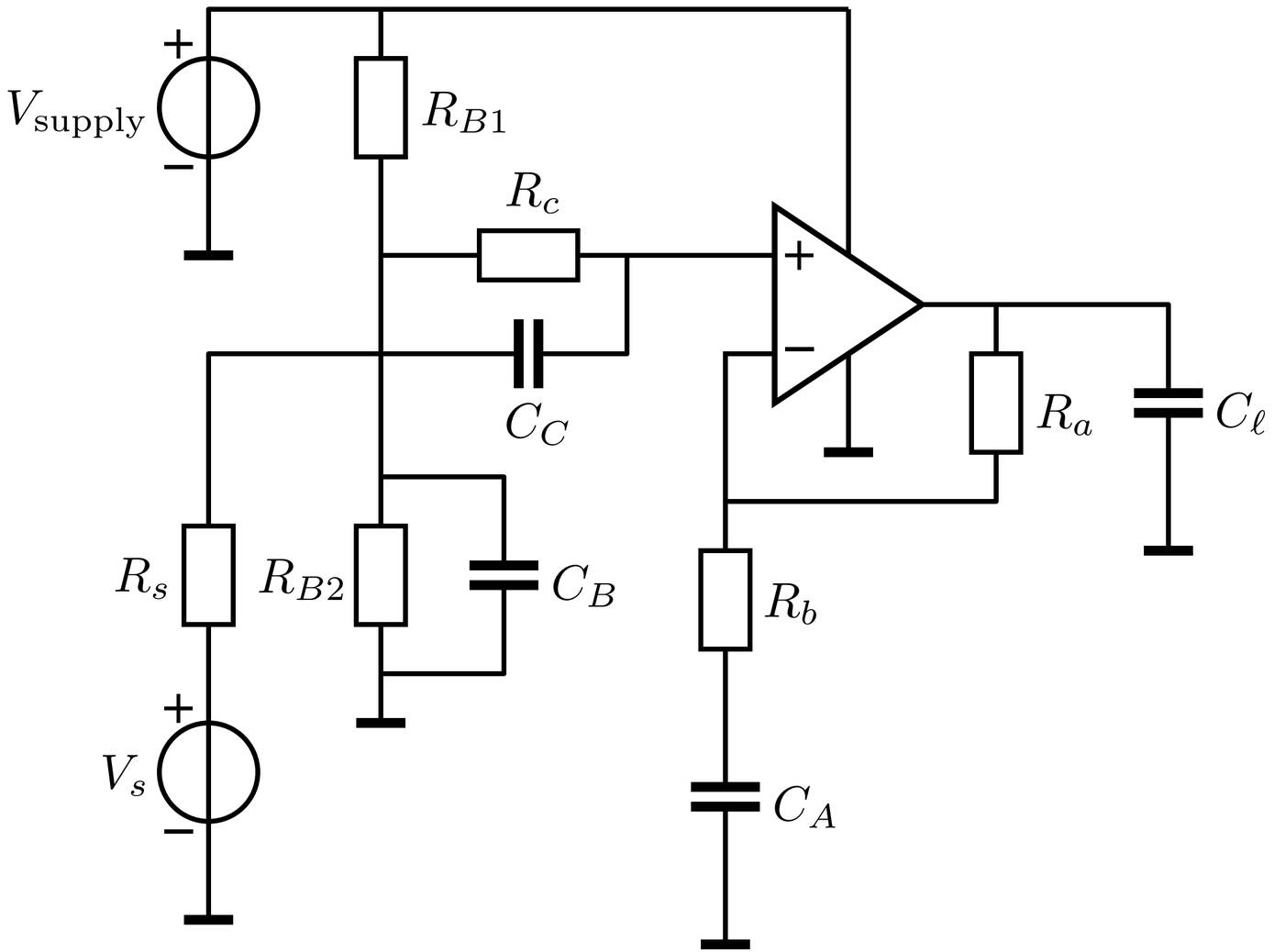
# Biasing errors

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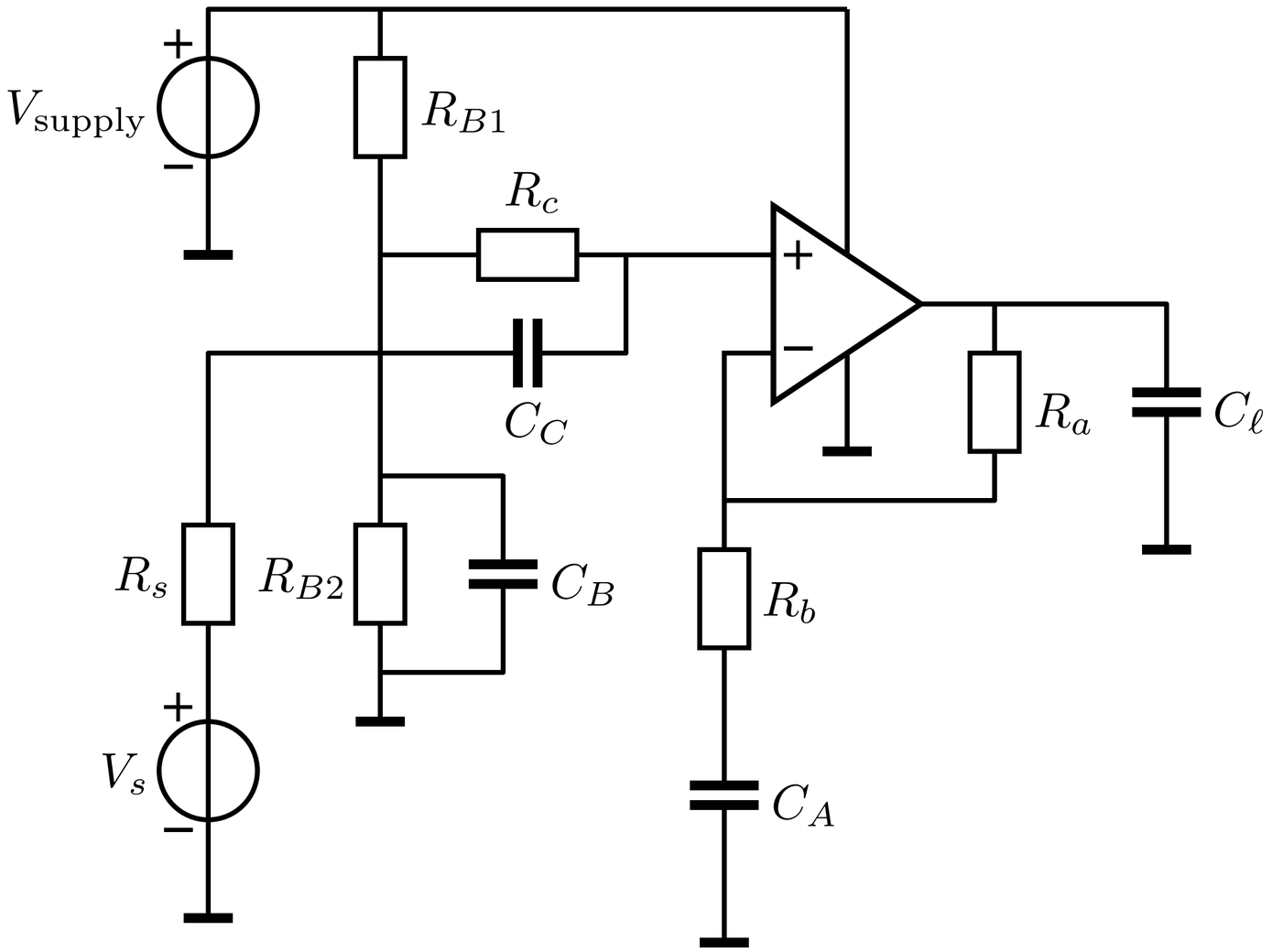


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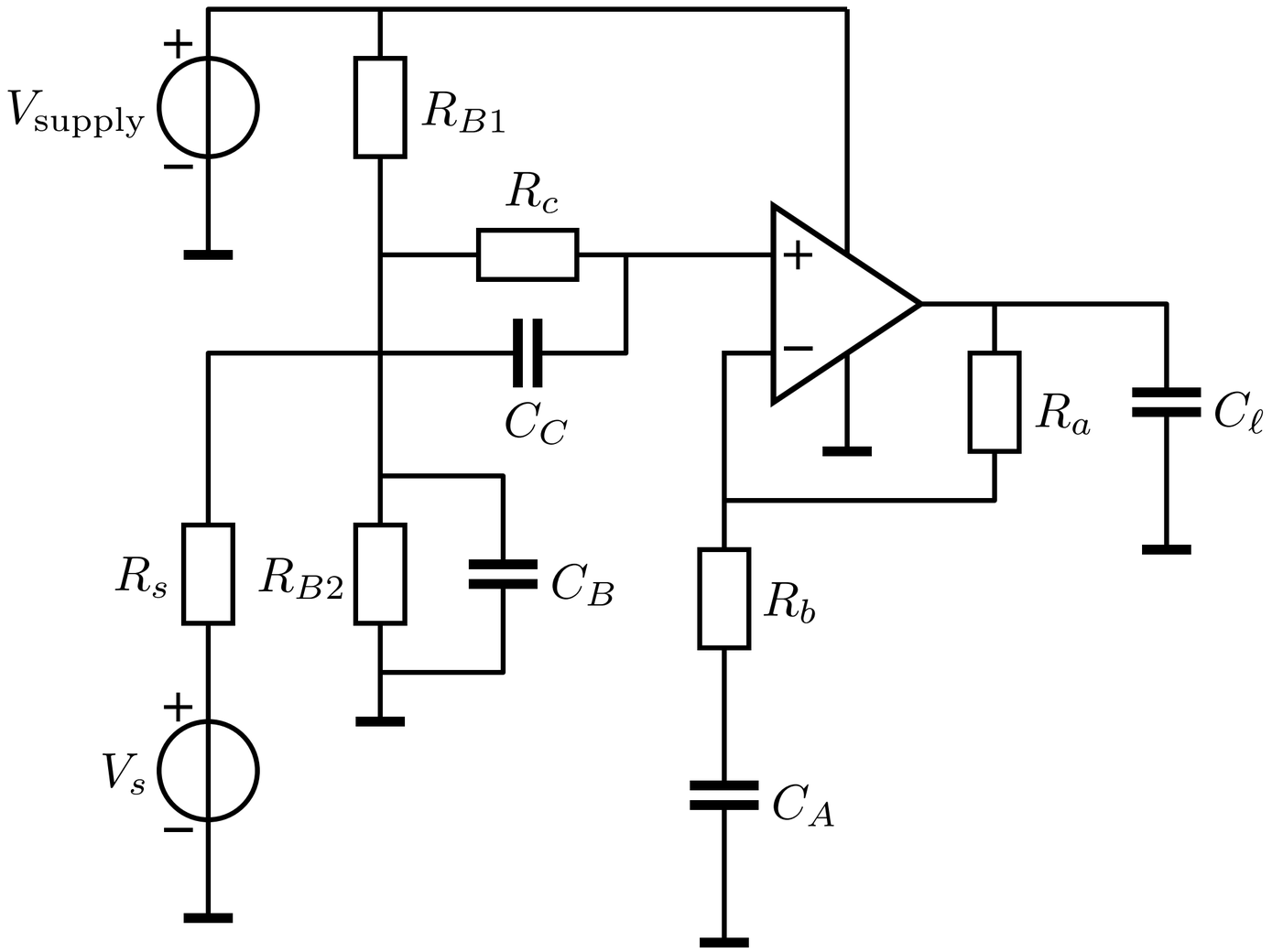


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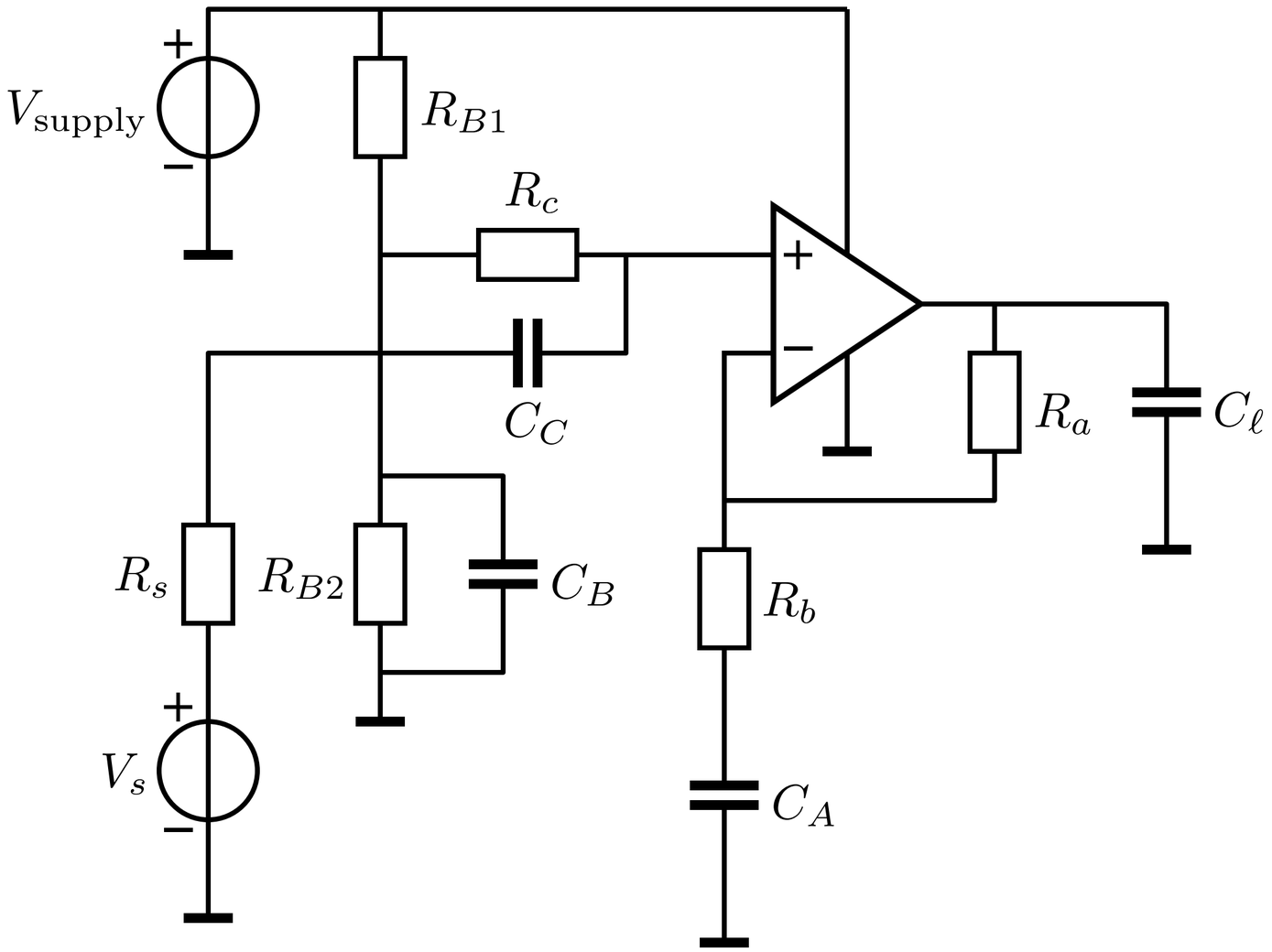


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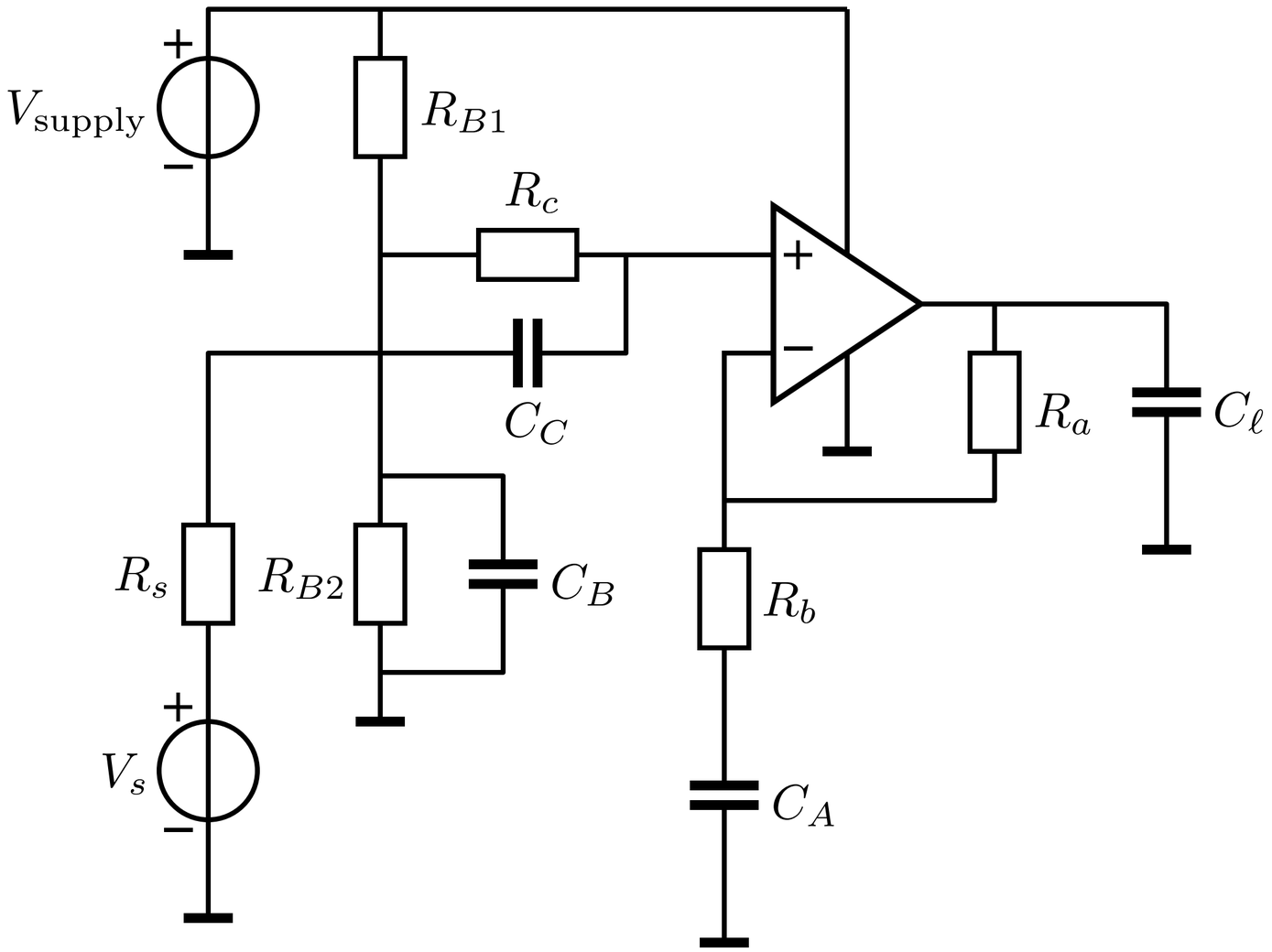


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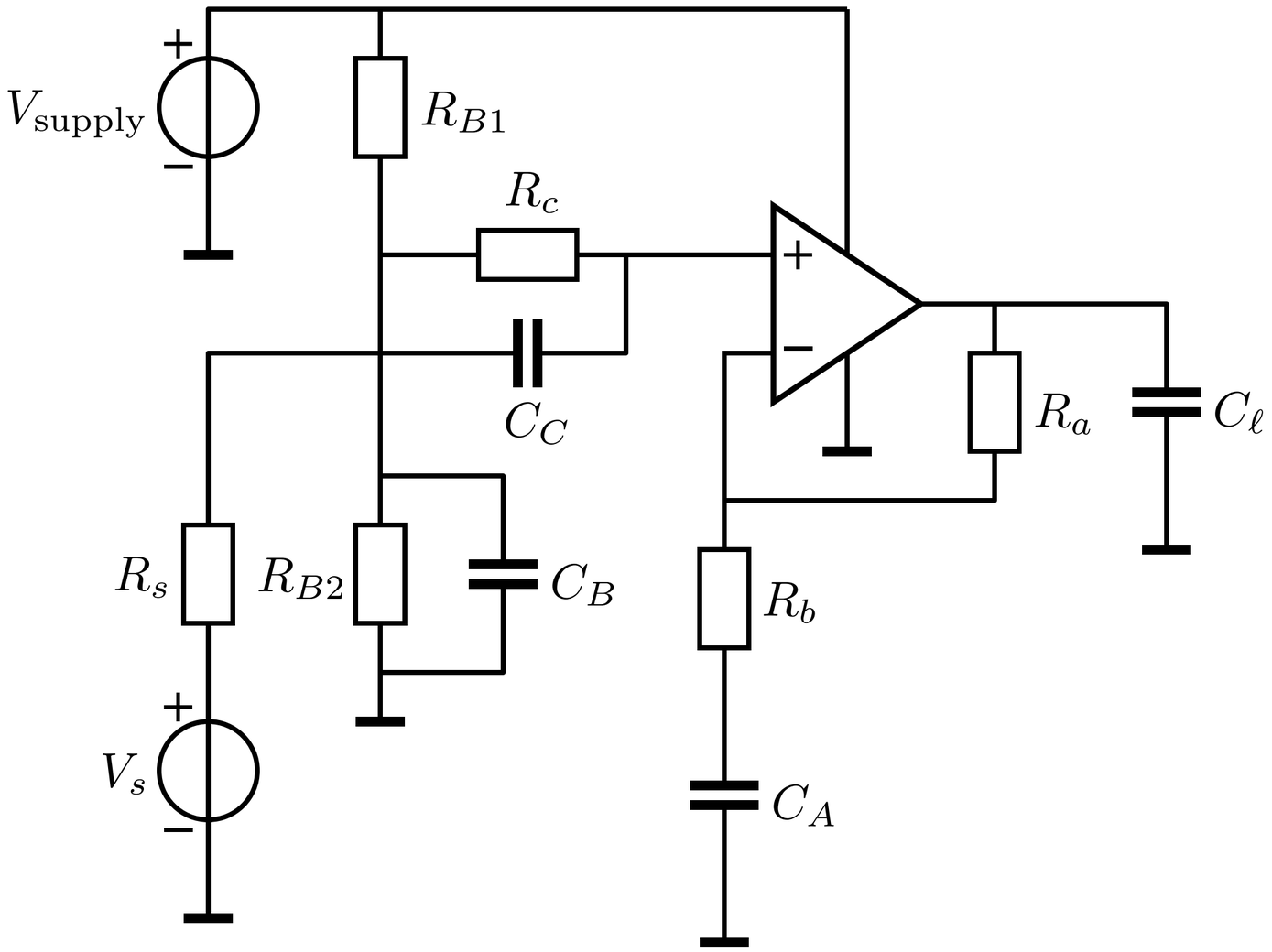


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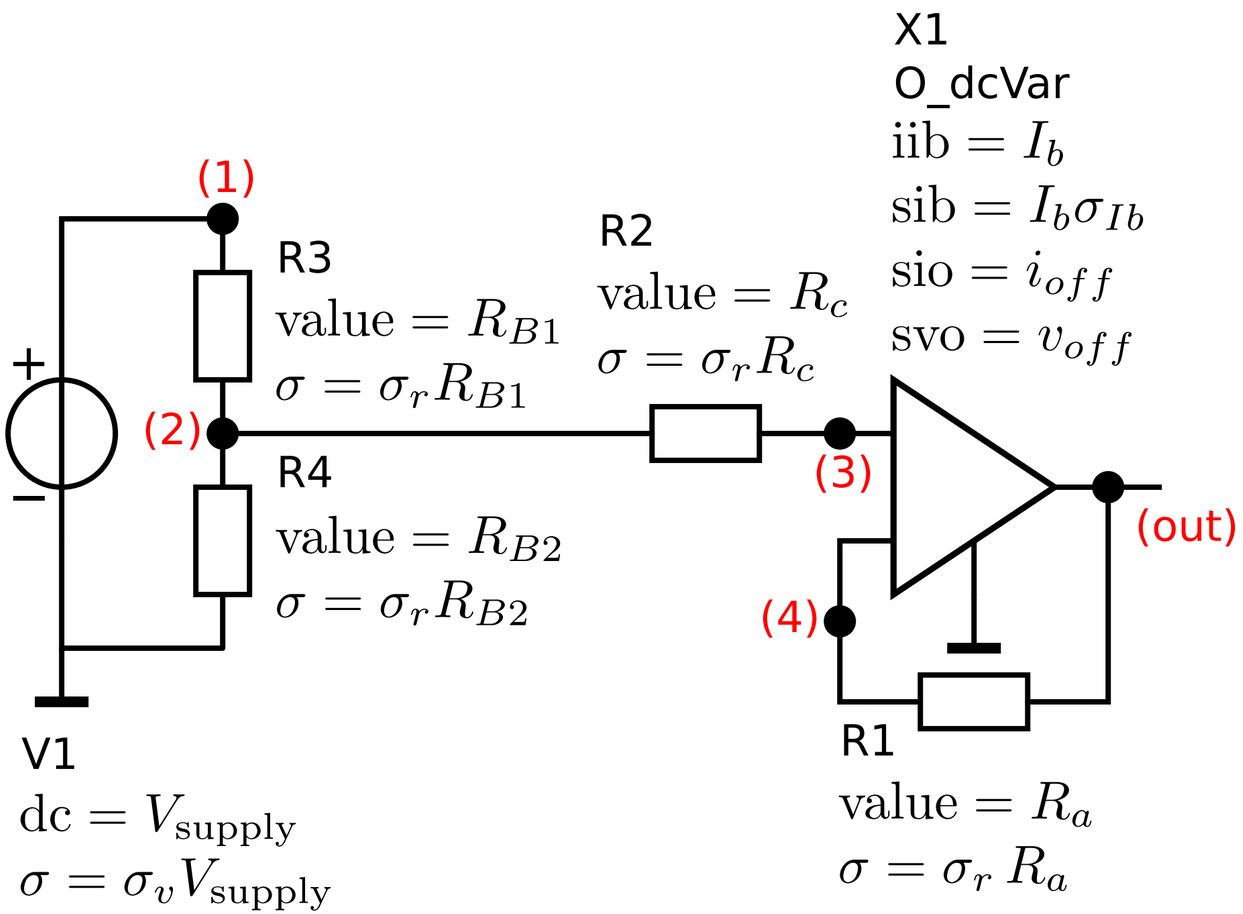

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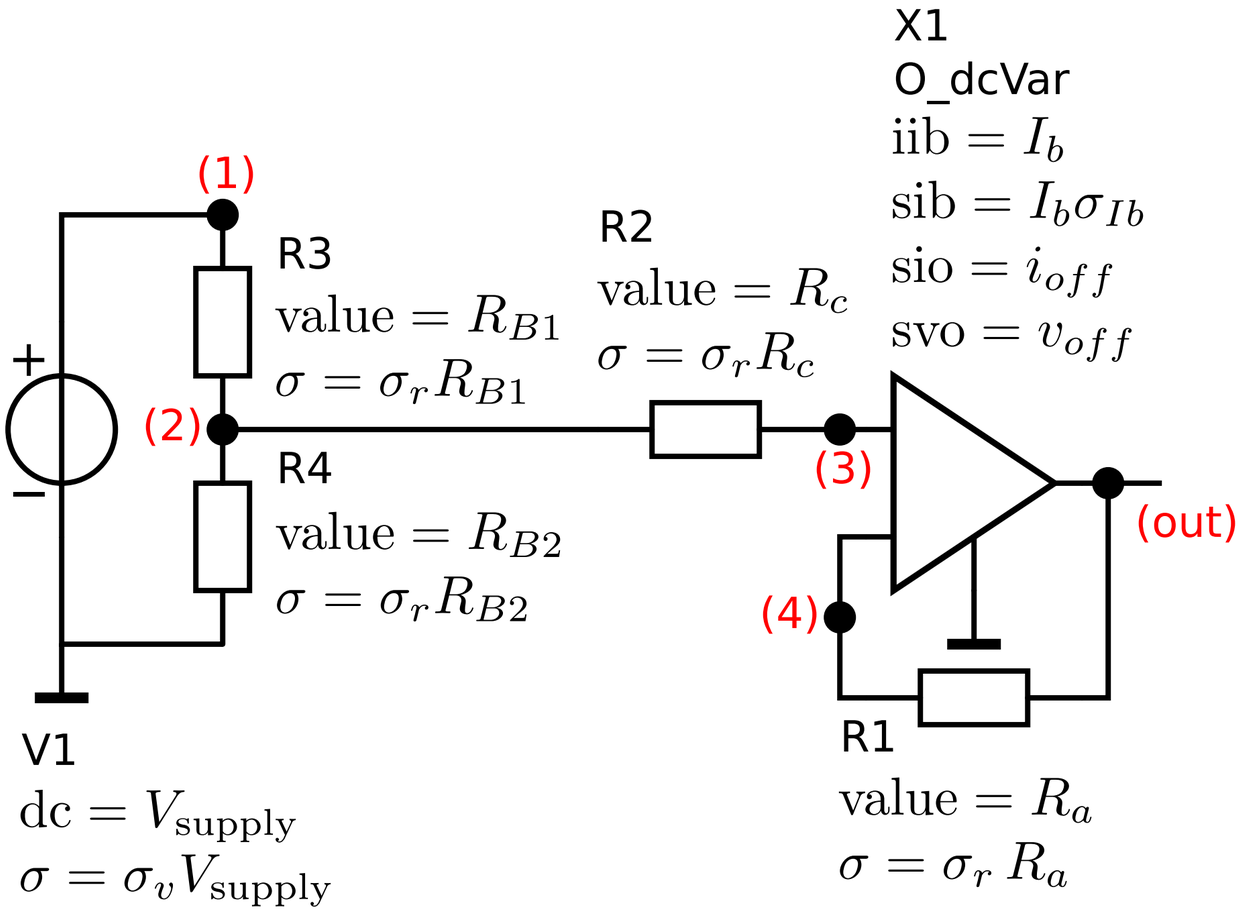


Simplified result: $R_c \gg \frac{R_{B1}R_{B2}}{R_{B1}+R_{B2}}$

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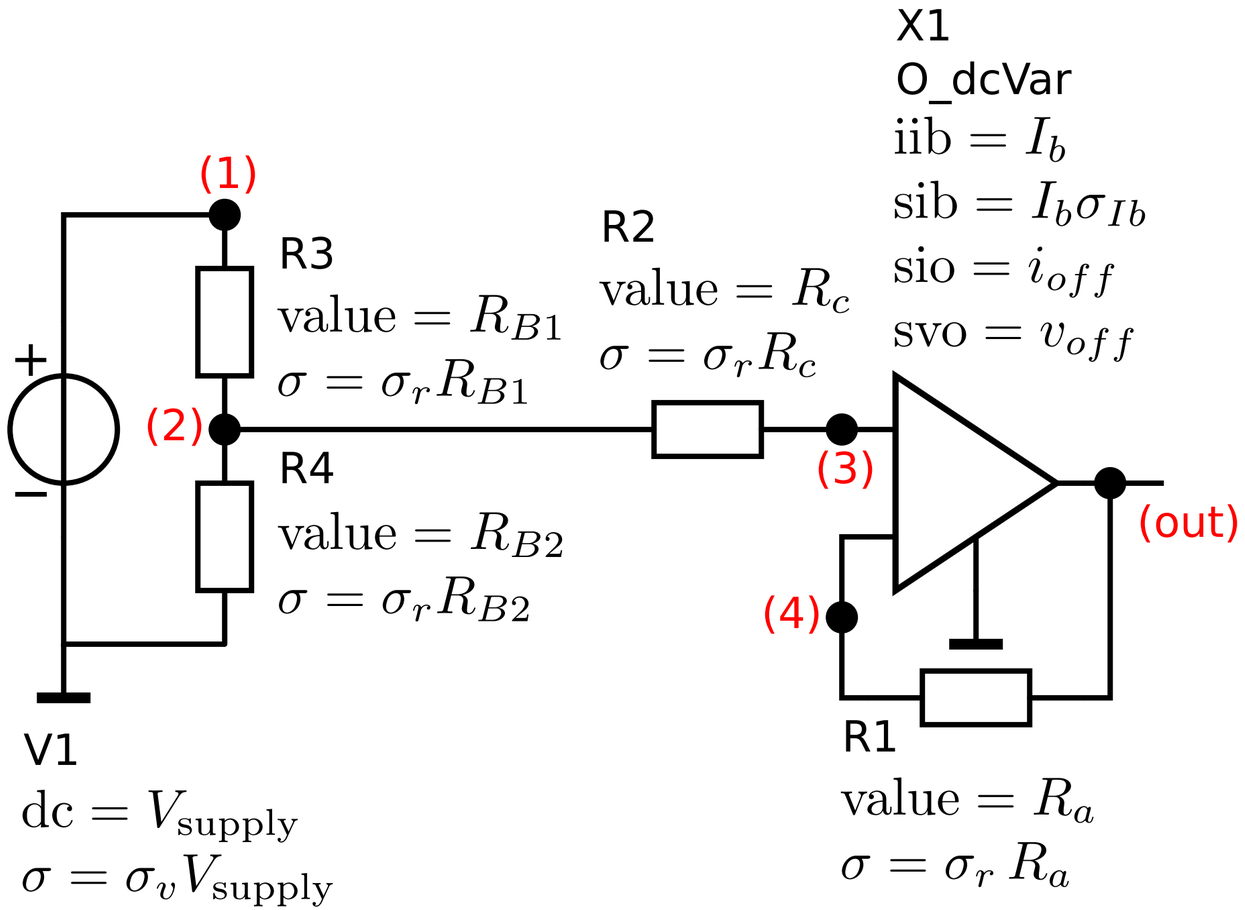


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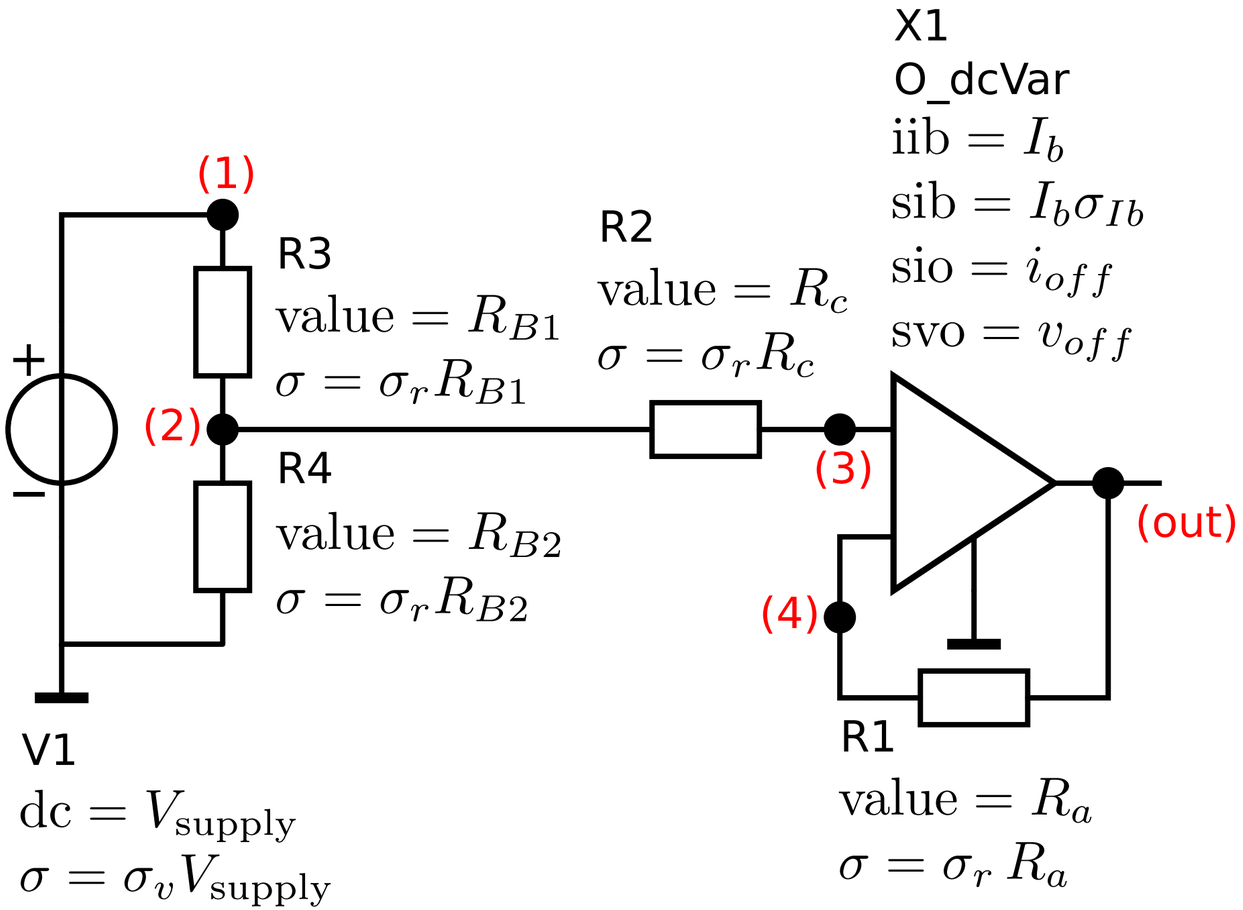


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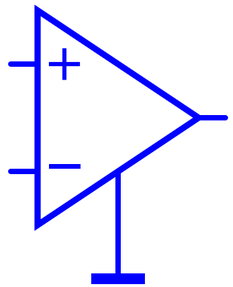


 

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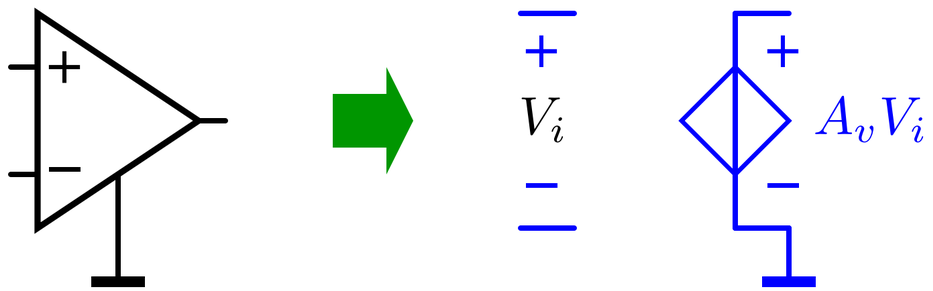

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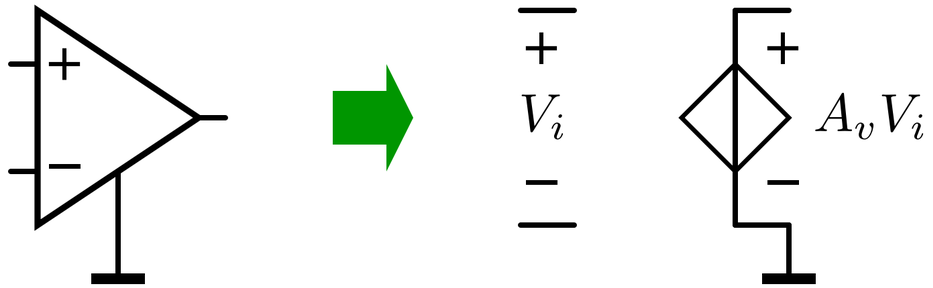

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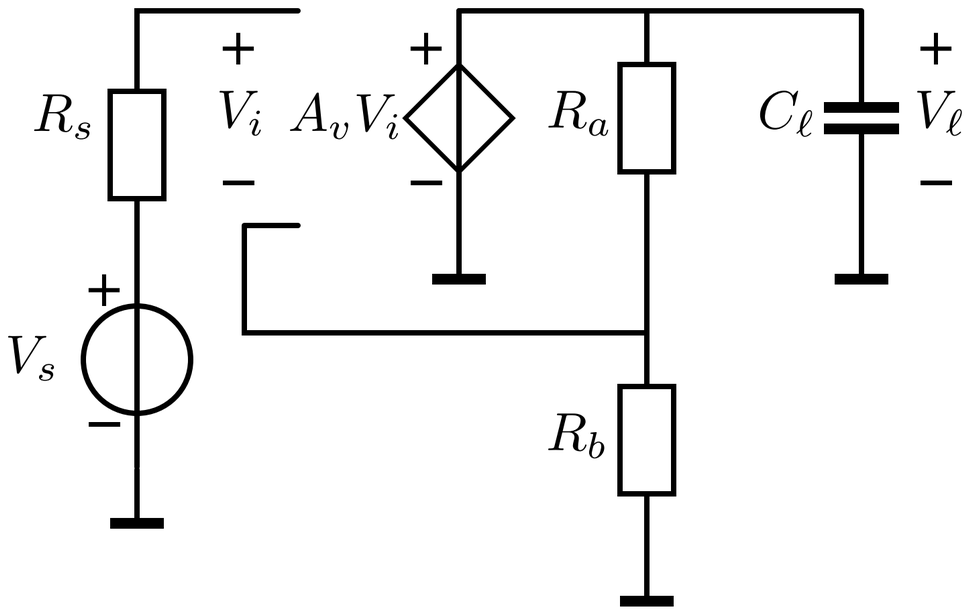

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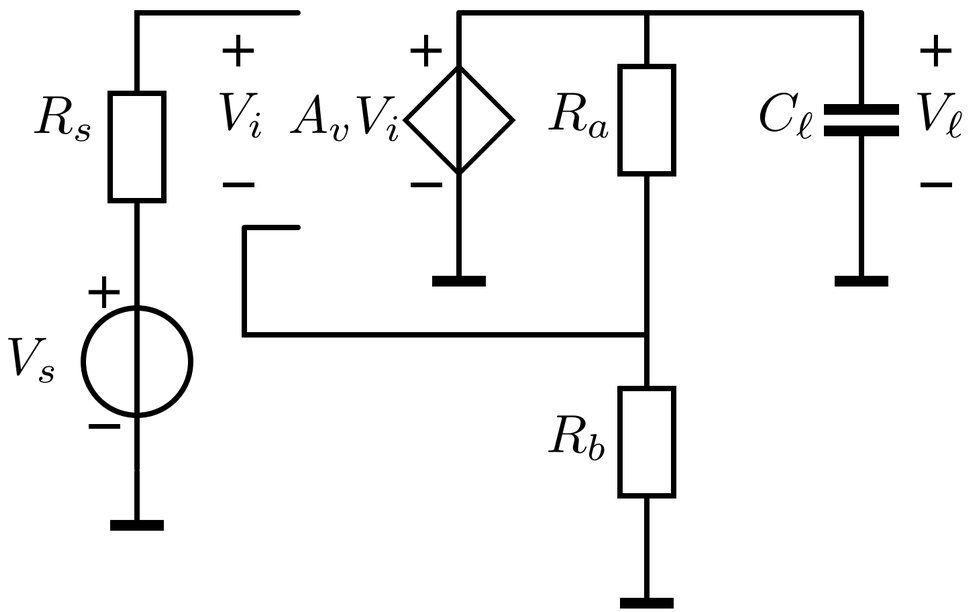


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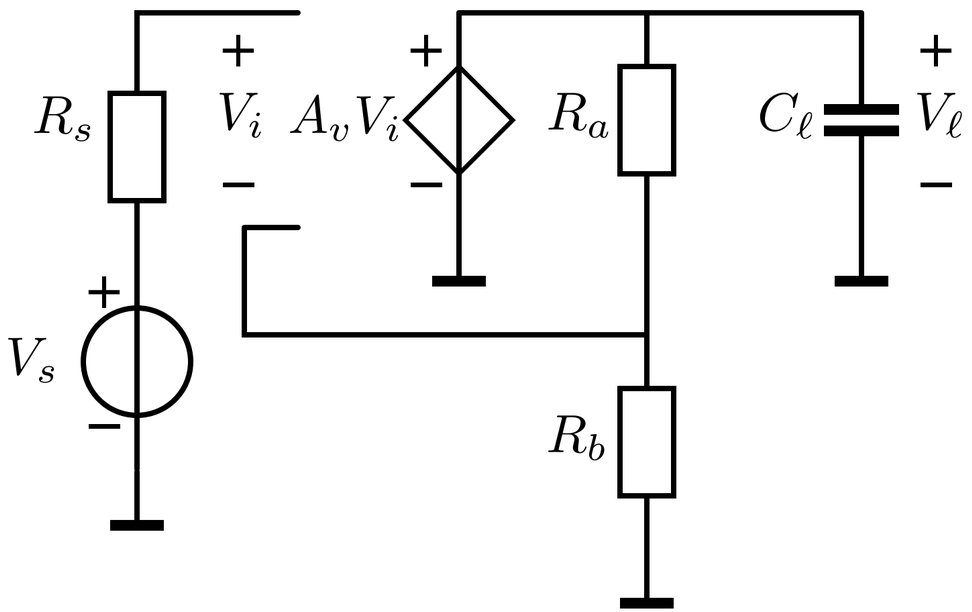


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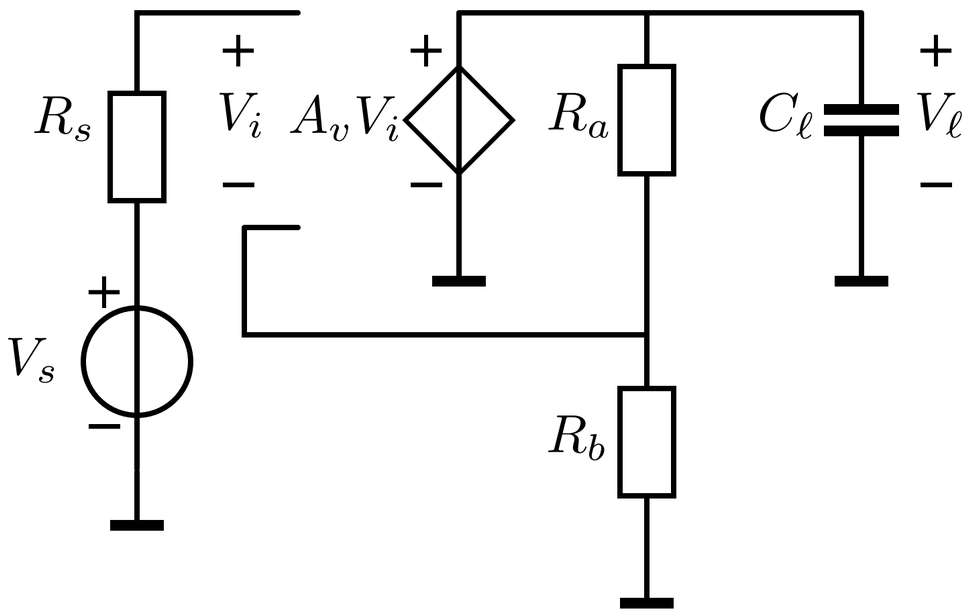


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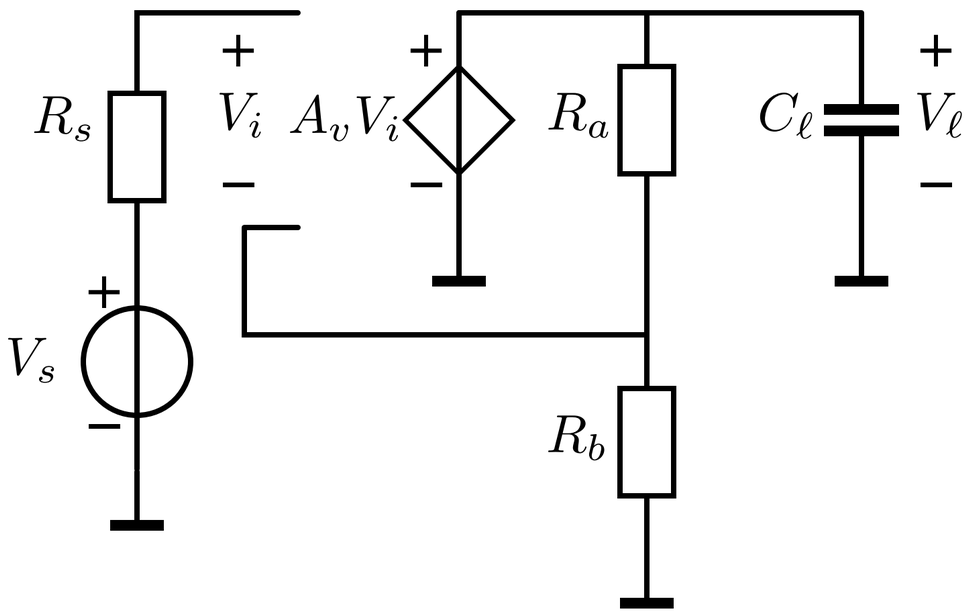


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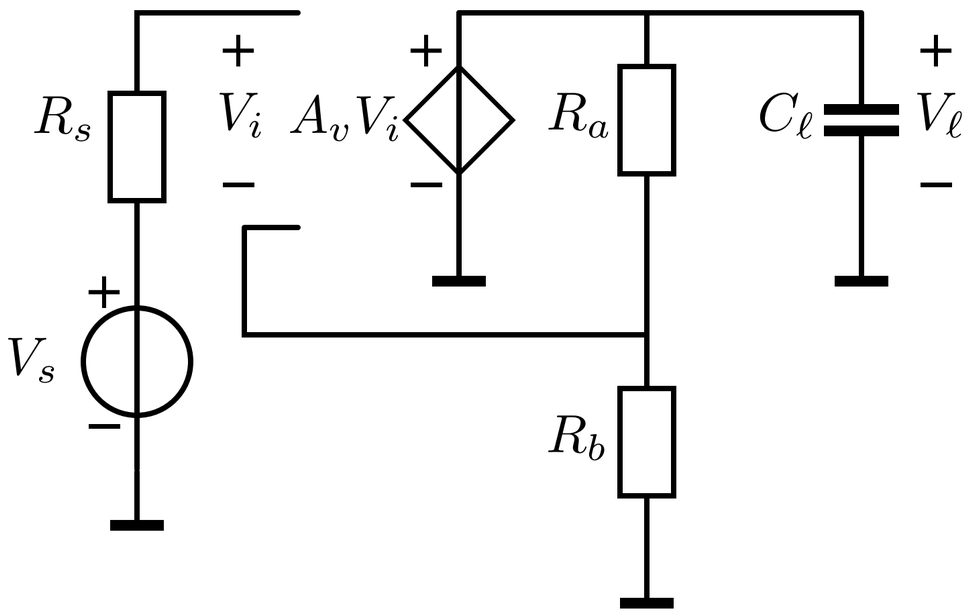


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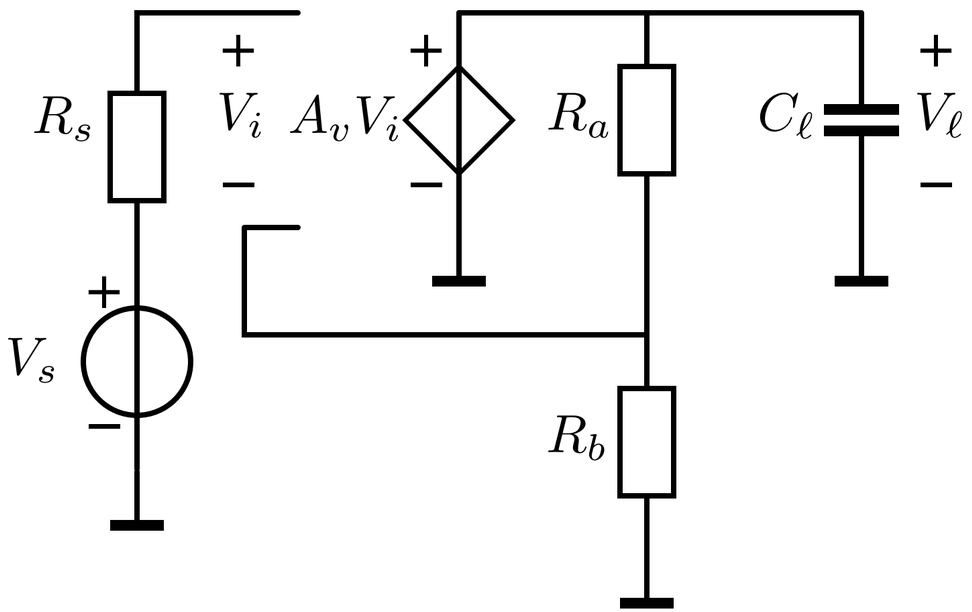


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