Structured Electronic Design
Amplifiers: Modeling of Ideal Behavior

Two-port model

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Functional model:
the power port will be omitted

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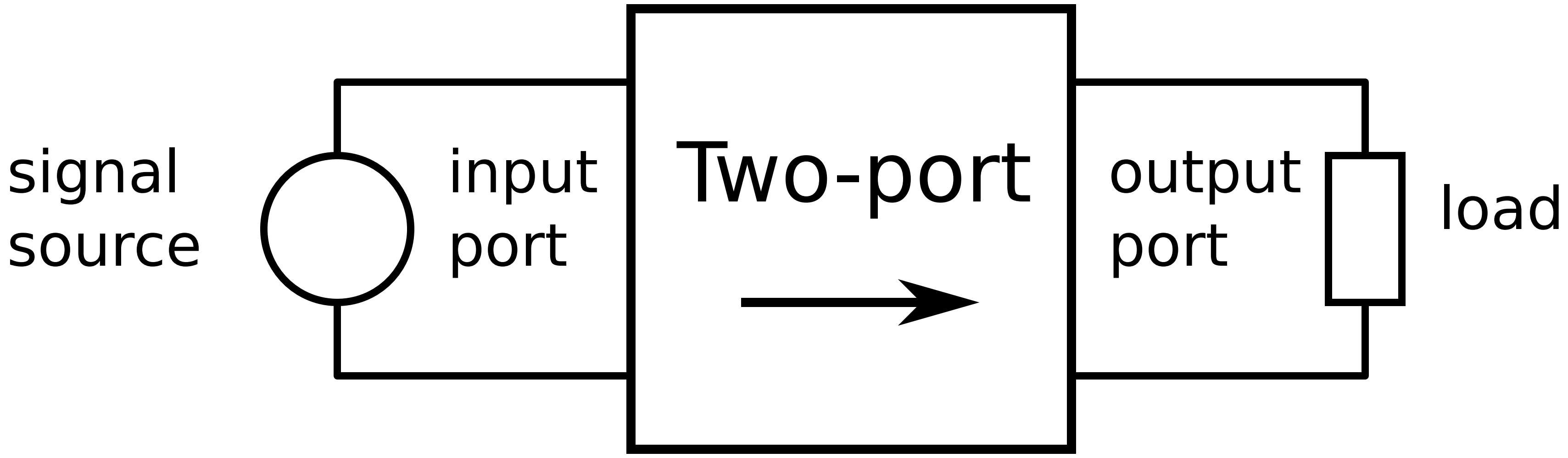

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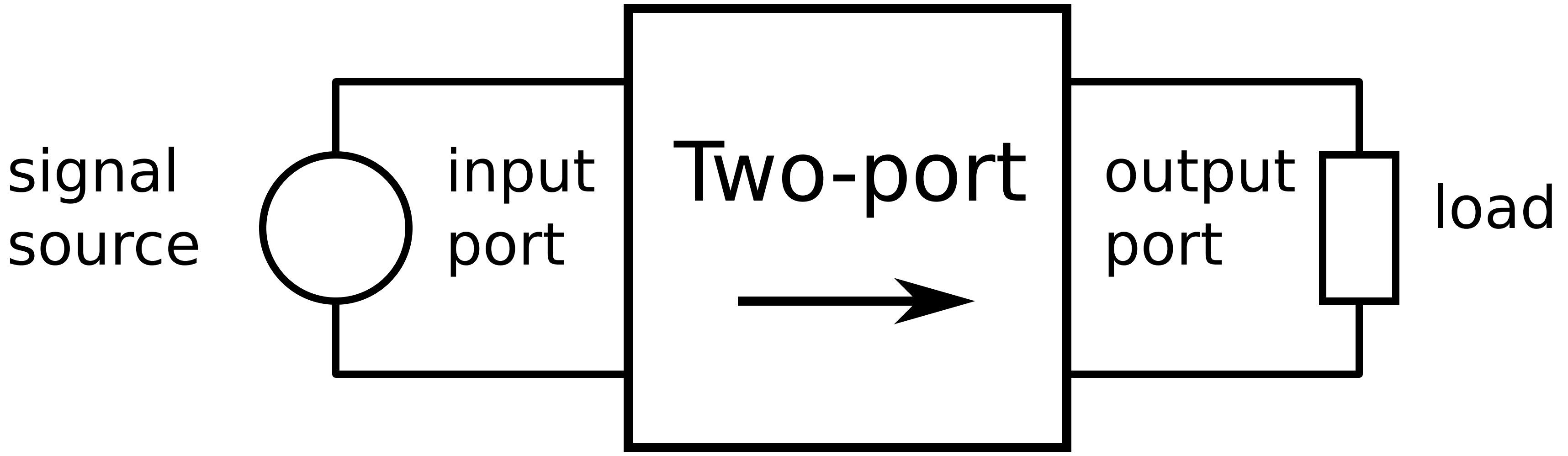
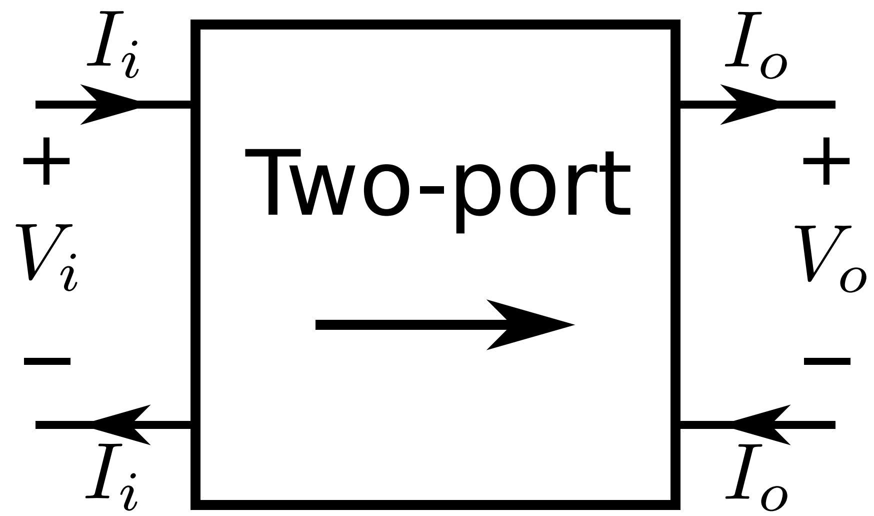


Two-port modeling: Chapter 18.6



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representations

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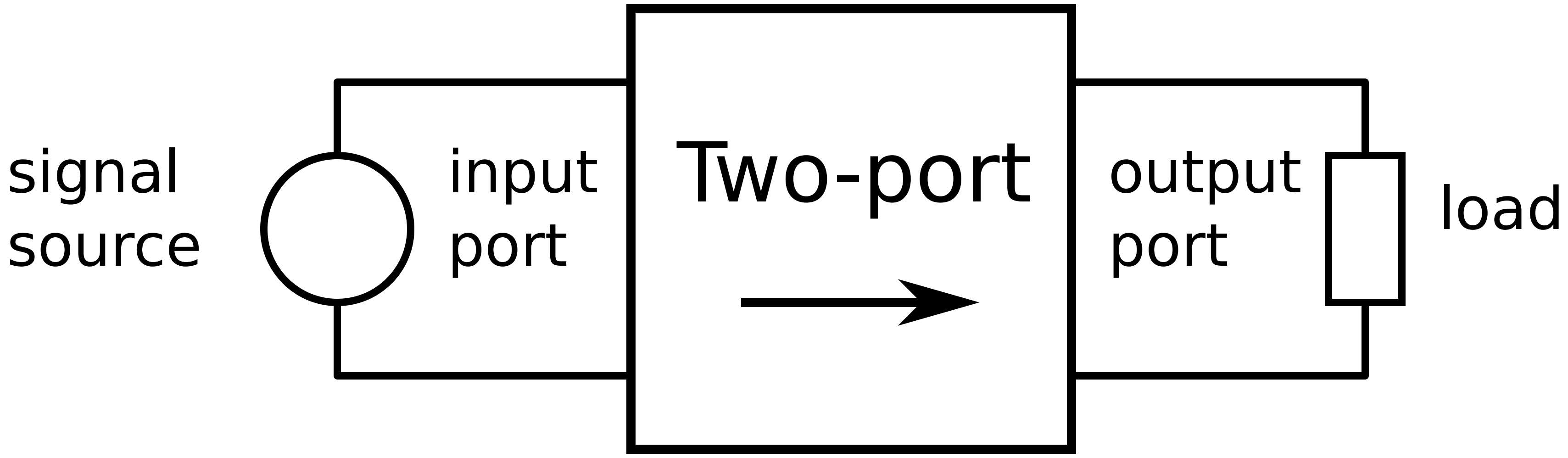

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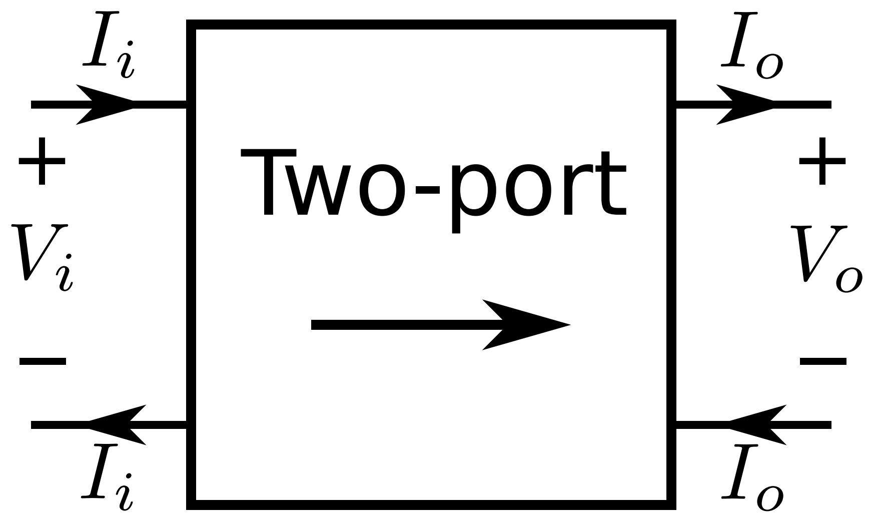

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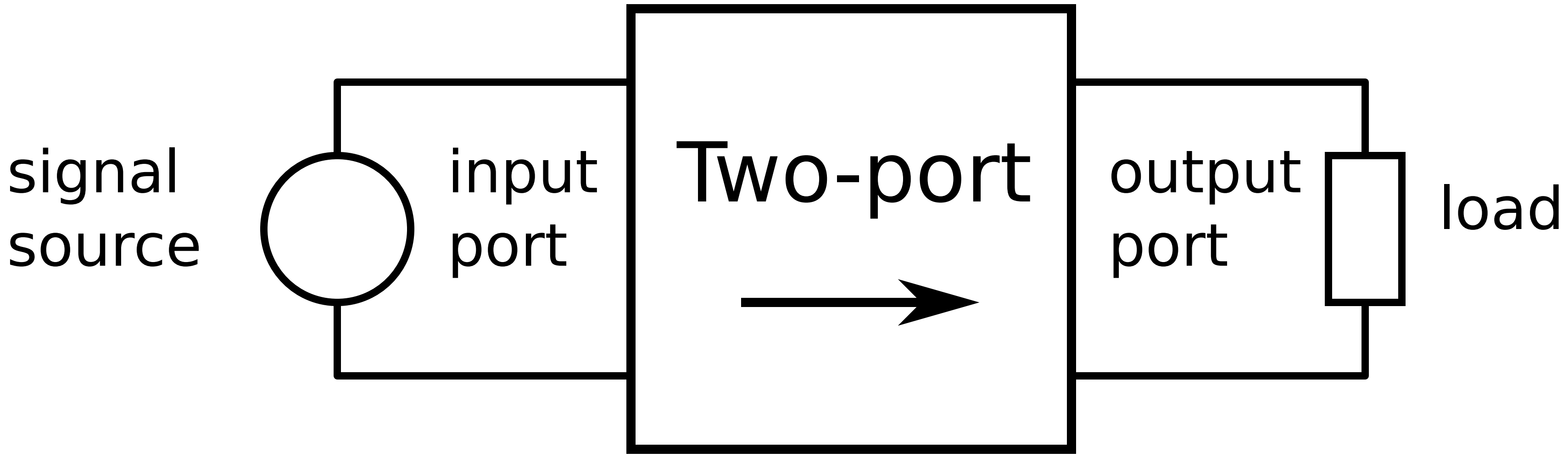

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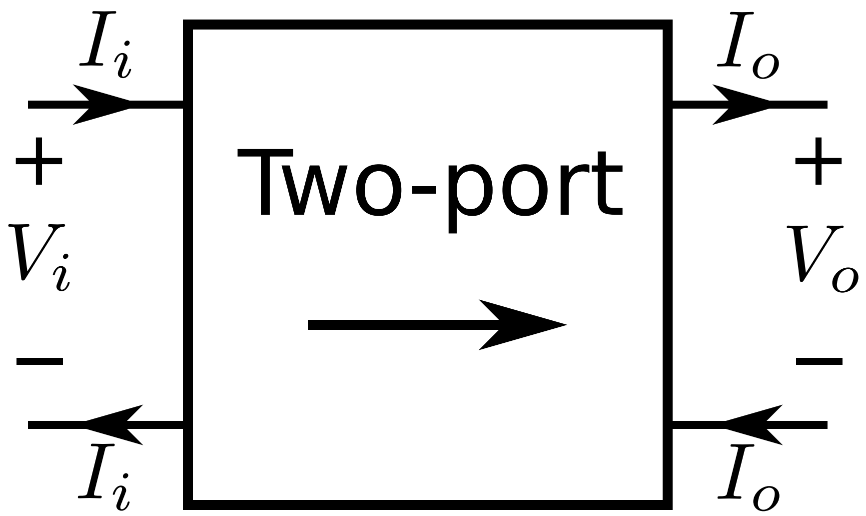

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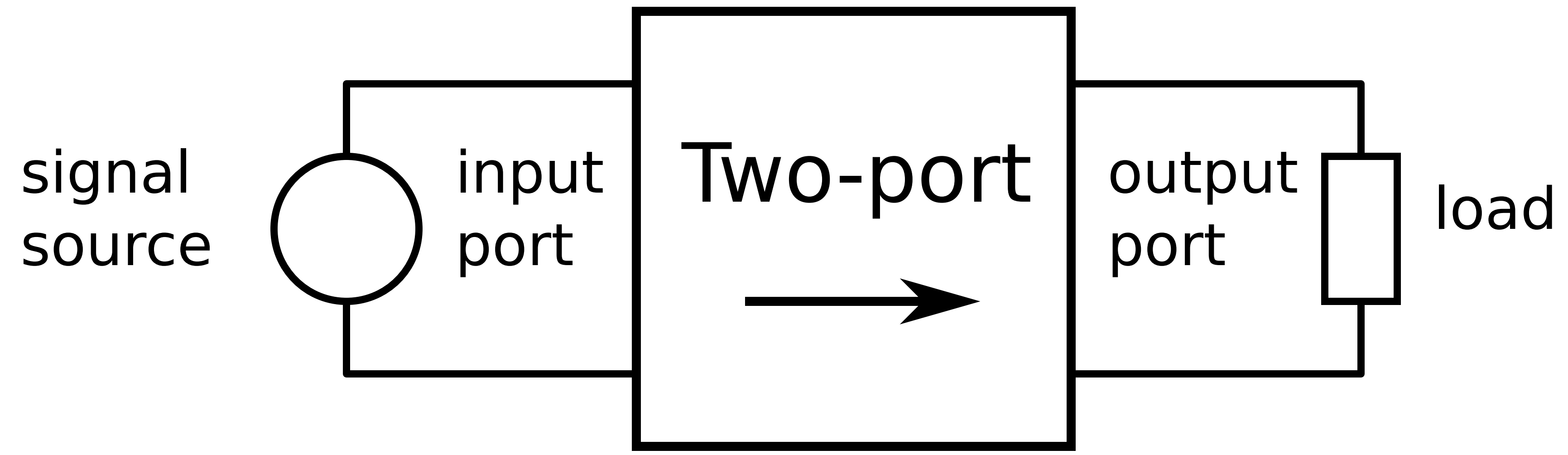

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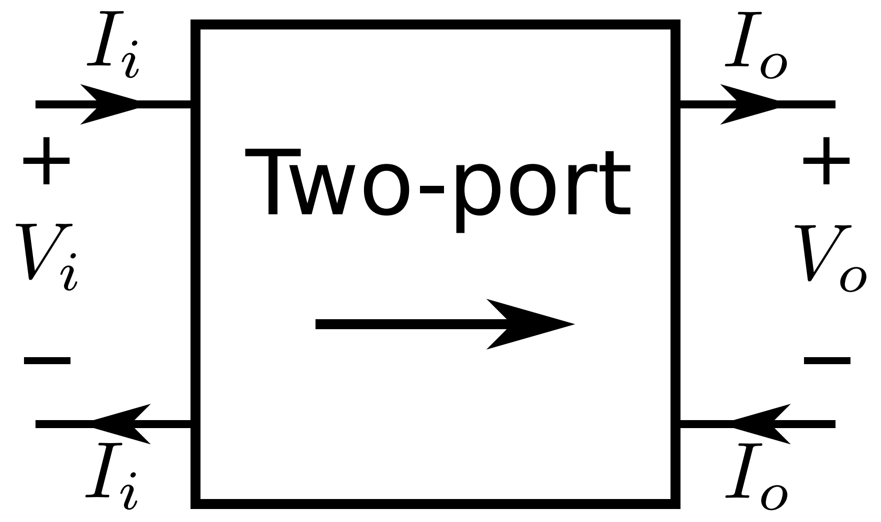

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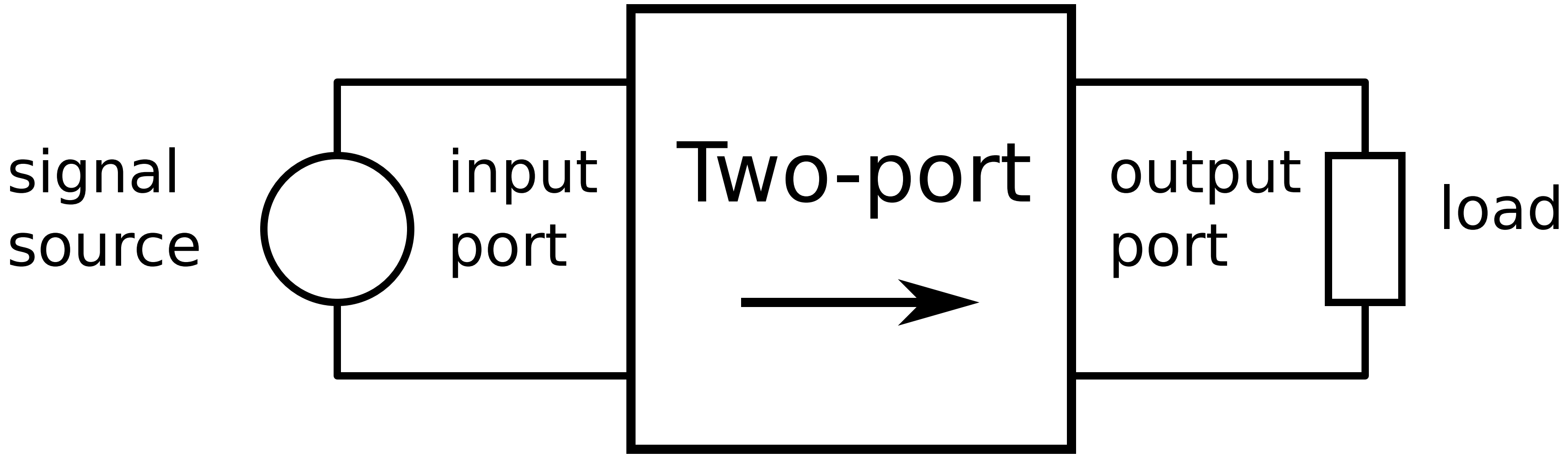

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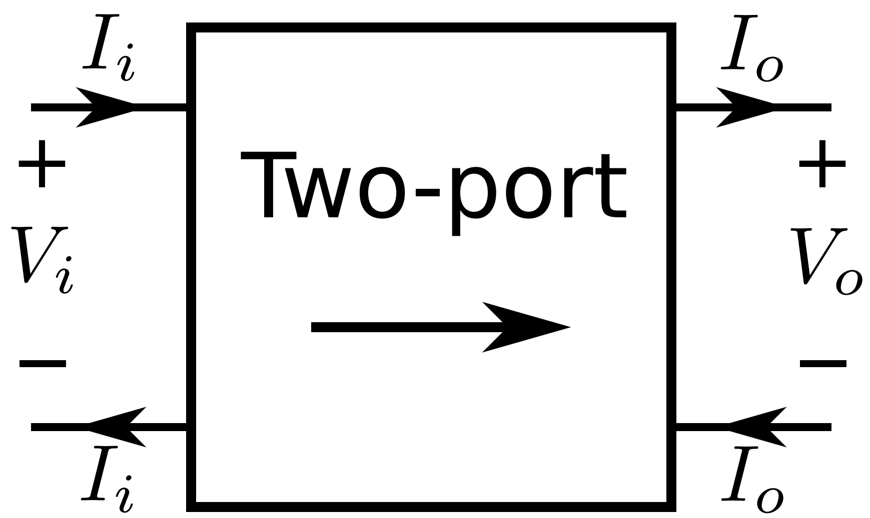

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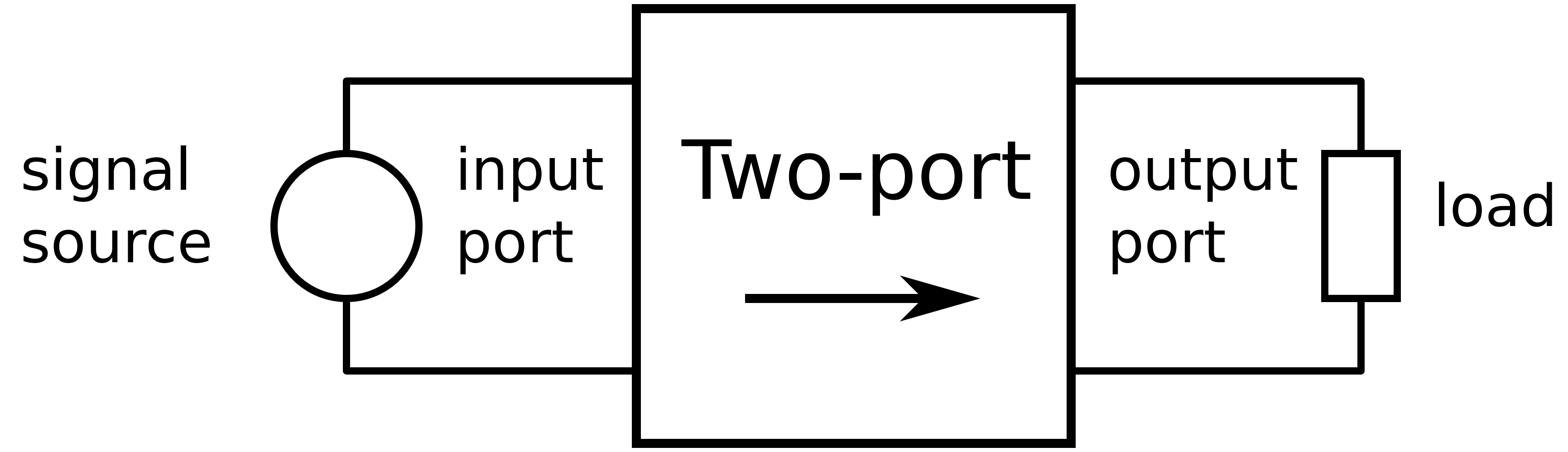

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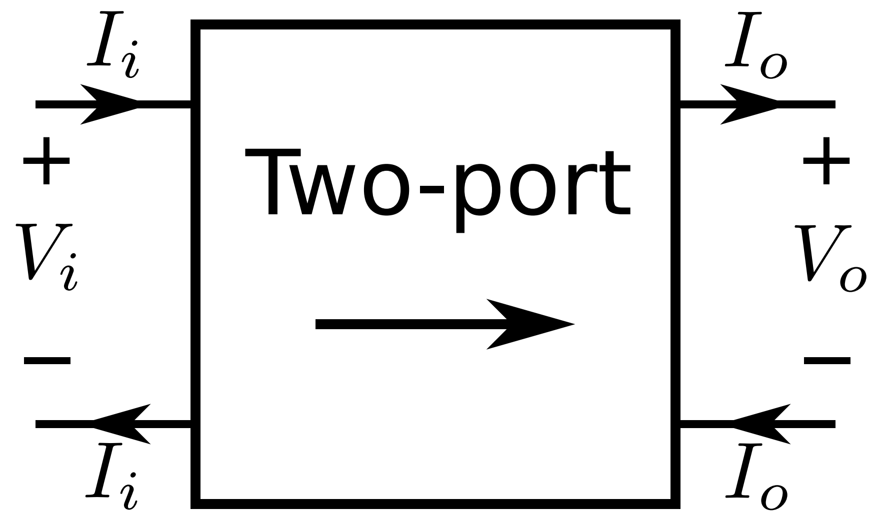

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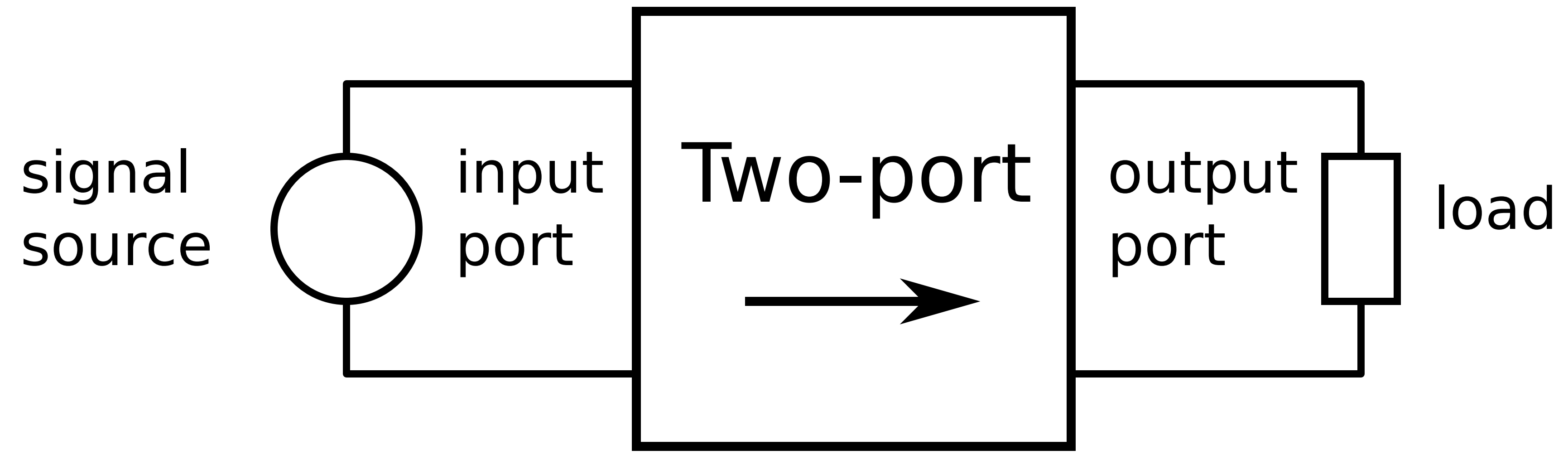

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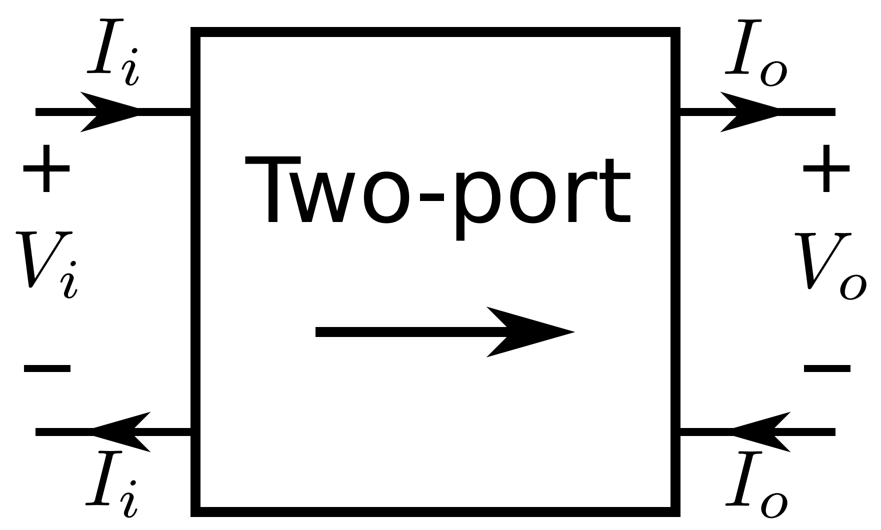

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$$C = \frac{1}{\zeta} = \left.\frac{I_i}{V_o}\right|_{I_o=0}, \qquad \text{Open output}$$

$$D = \frac{1}{\alpha} = \left.\frac{I_i}{I_o}\right|_{V_o=0}. \qquad \text{Shorted output}$$

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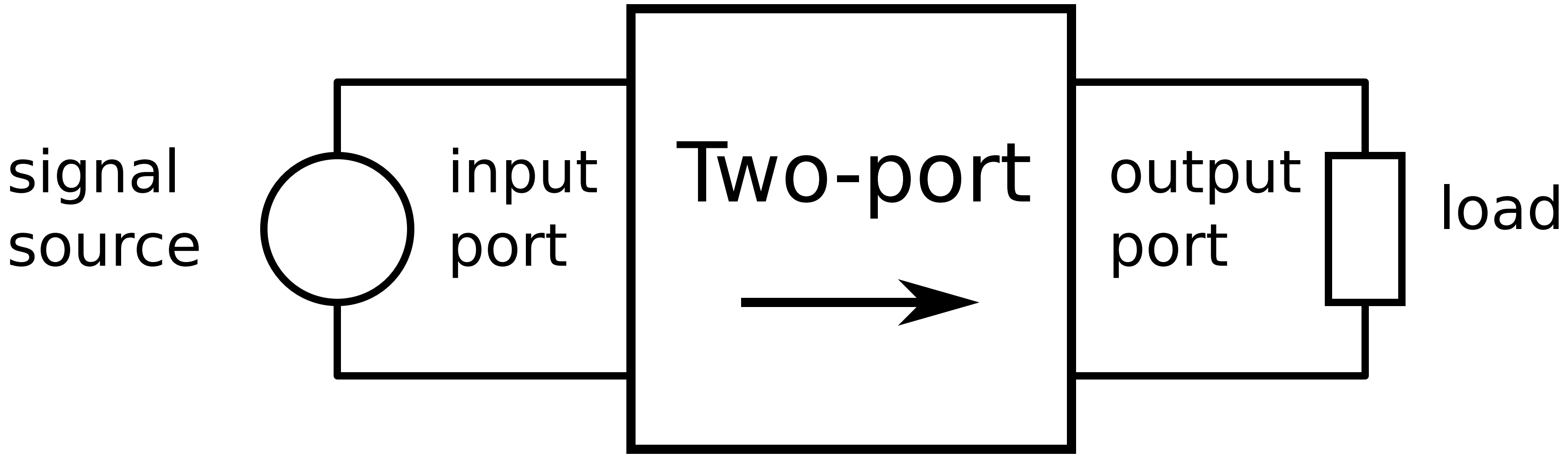

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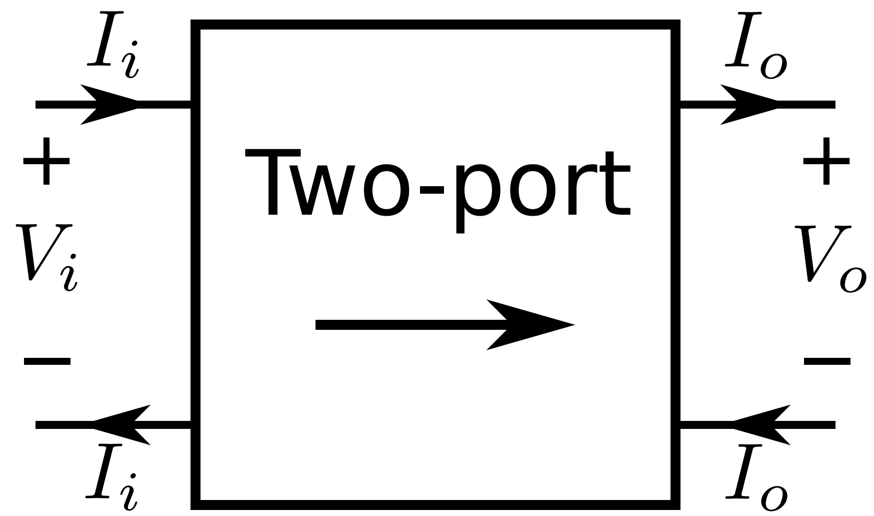

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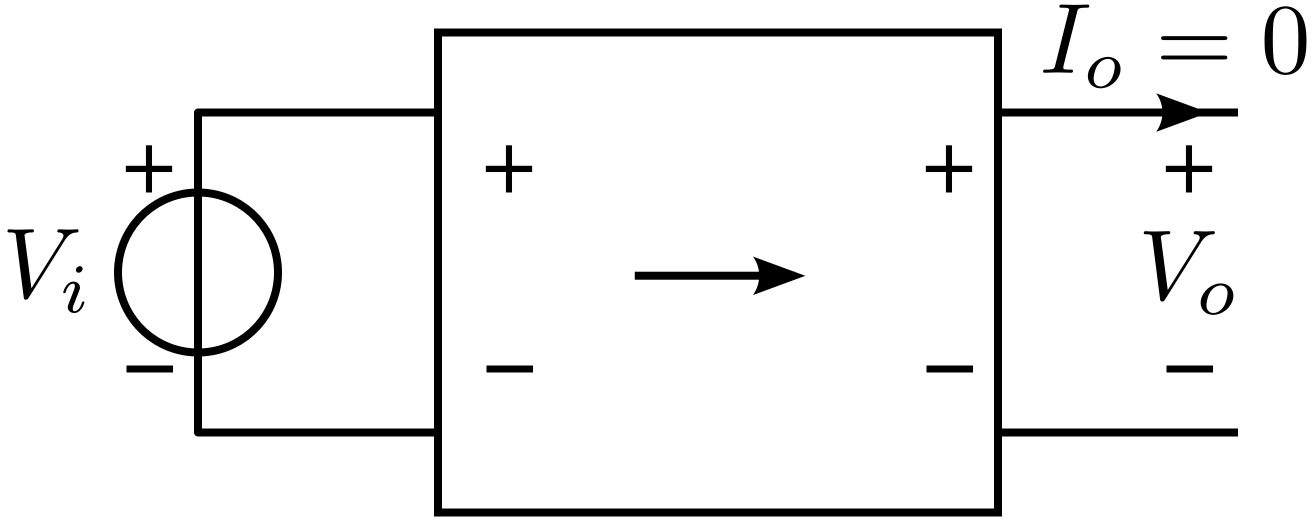
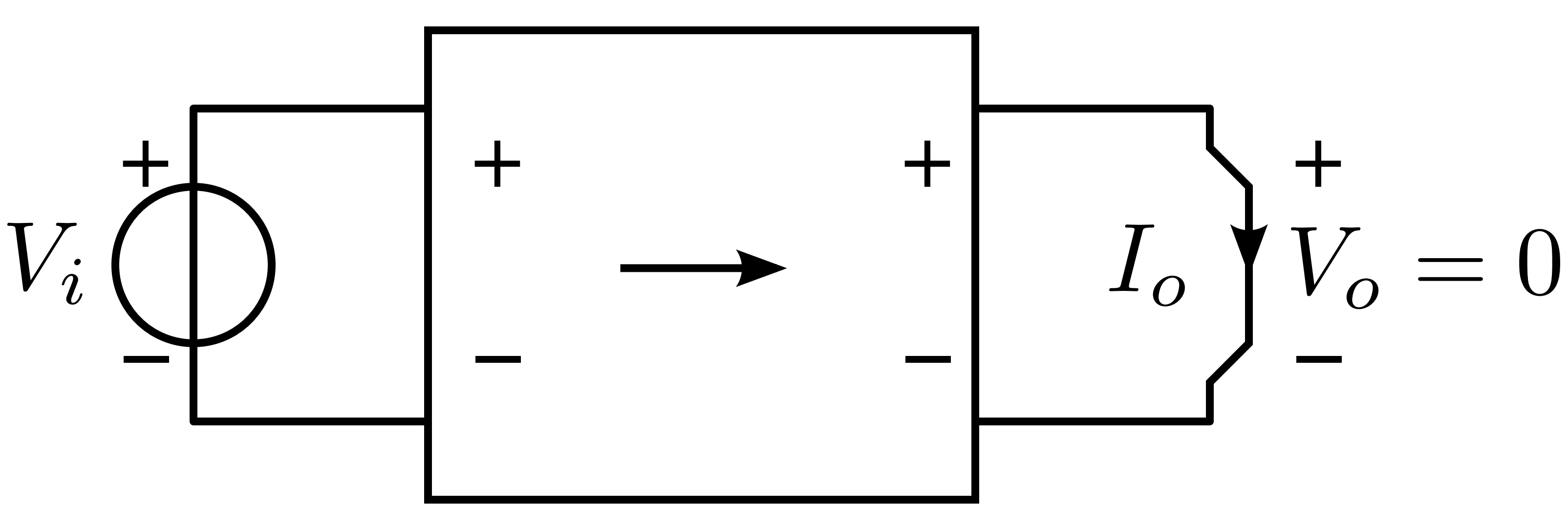
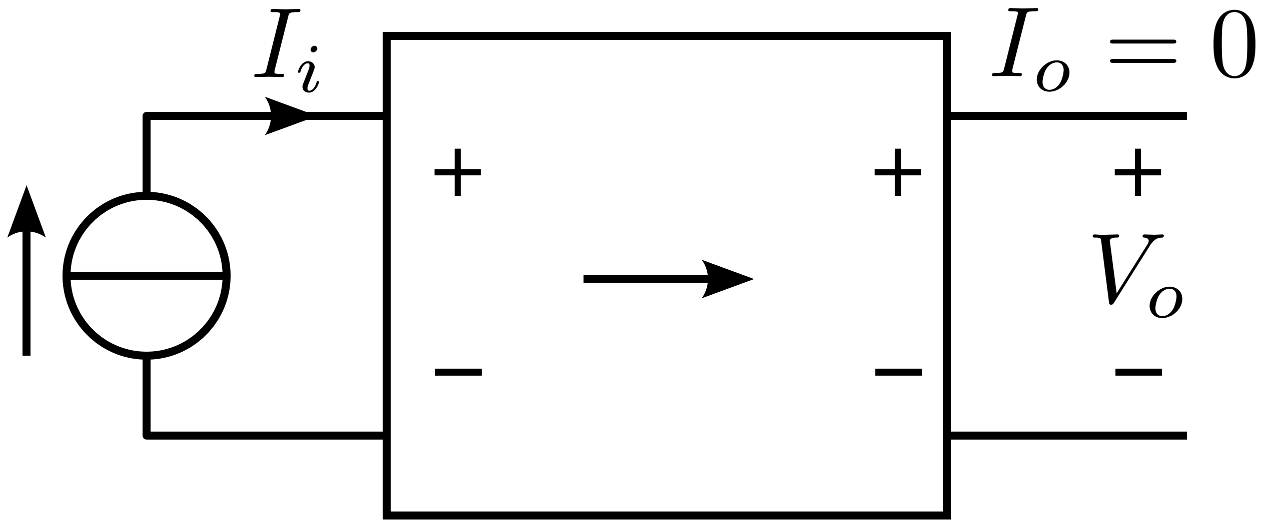
Determination of the transmission-1 two-port parameters



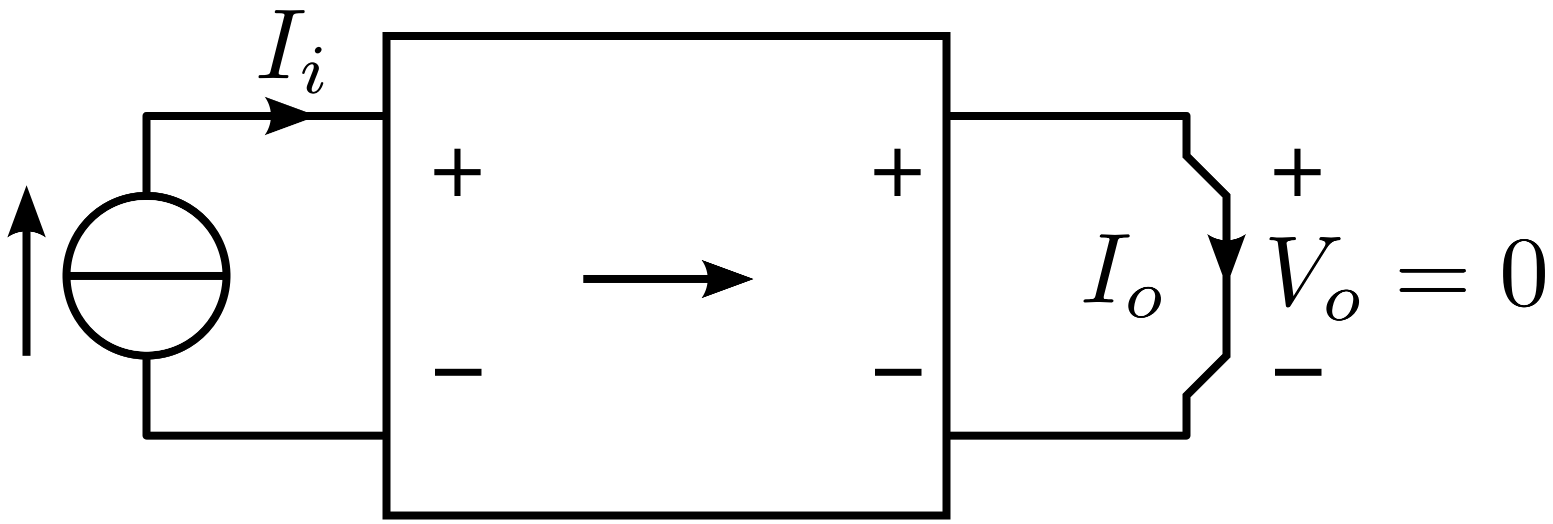
$$\mu = \frac{1}{A} = \left.\frac{V_o}{V_i}\right|_{I_o=0}$$



$$\gamma = \frac{1}{B} = \left.\frac{I_o}{V_i}\right|_{V_o=0}$$



$$\zeta = \frac{1}{C} = \left.\frac{V_o}{I_i}\right|_{I_o=0}$$



$$\alpha = \frac{1}{D} = \left.\frac{I_o}{I_i}\right|_{V_o=0}$$

Source to load transfer

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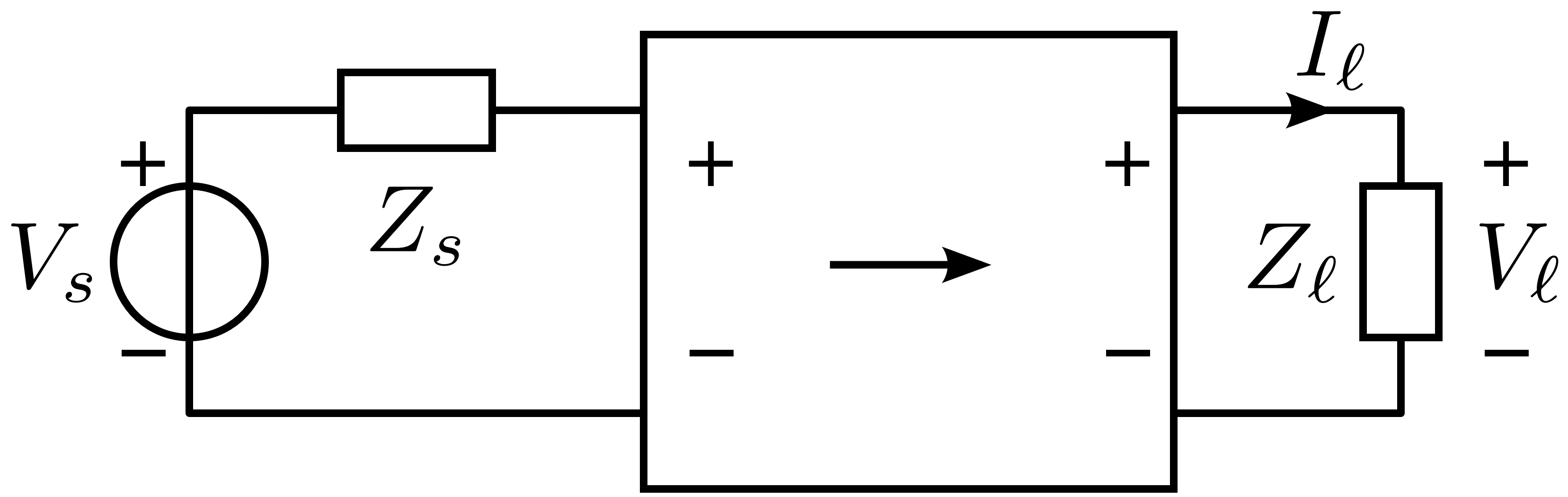
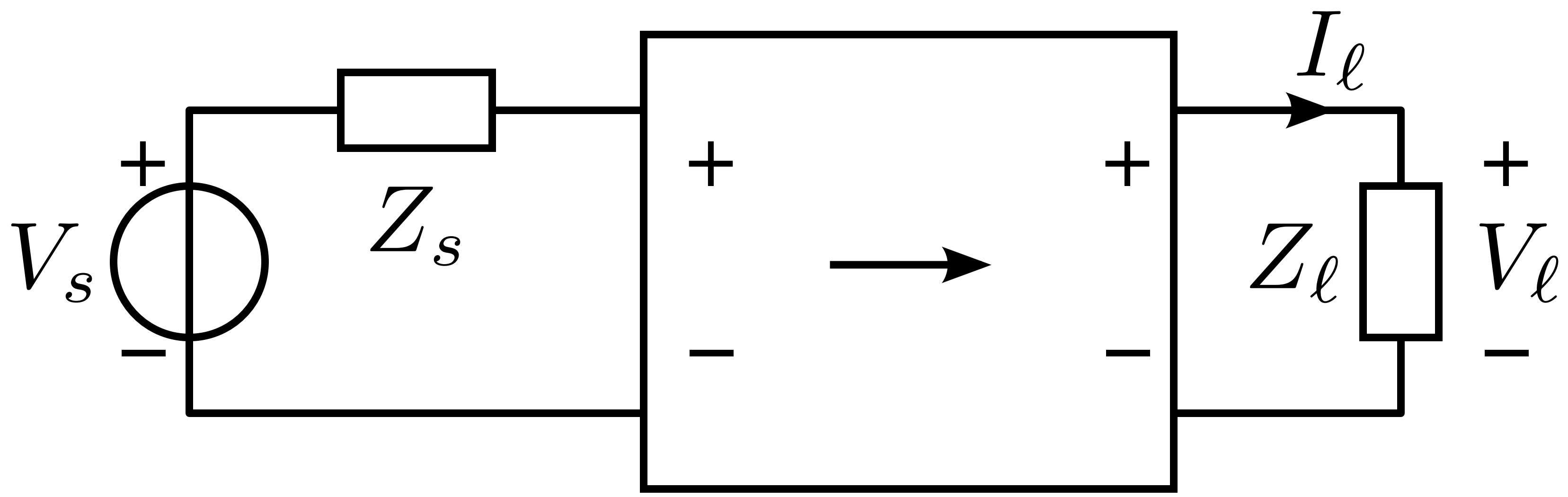


$$A_v = \frac{V_\ell}{V_s} = \frac{1}{A + B\frac{1}{Z_\ell} + C Z_s + D\frac{Z_s}{Z_\ell}}$$

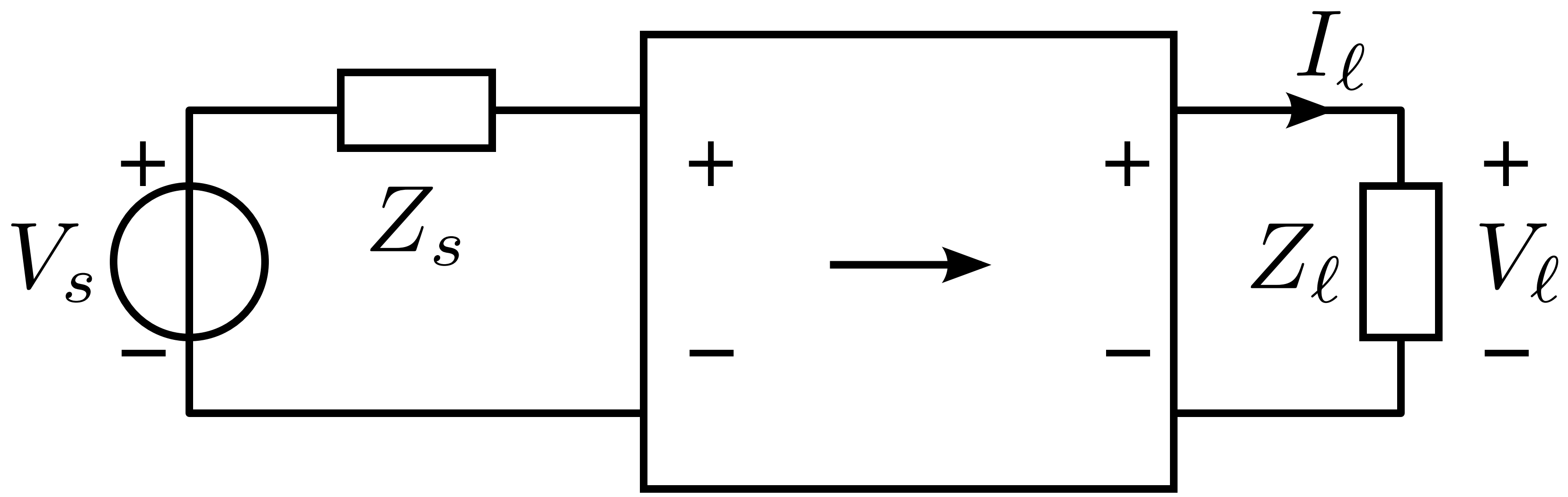
Source to load transfer

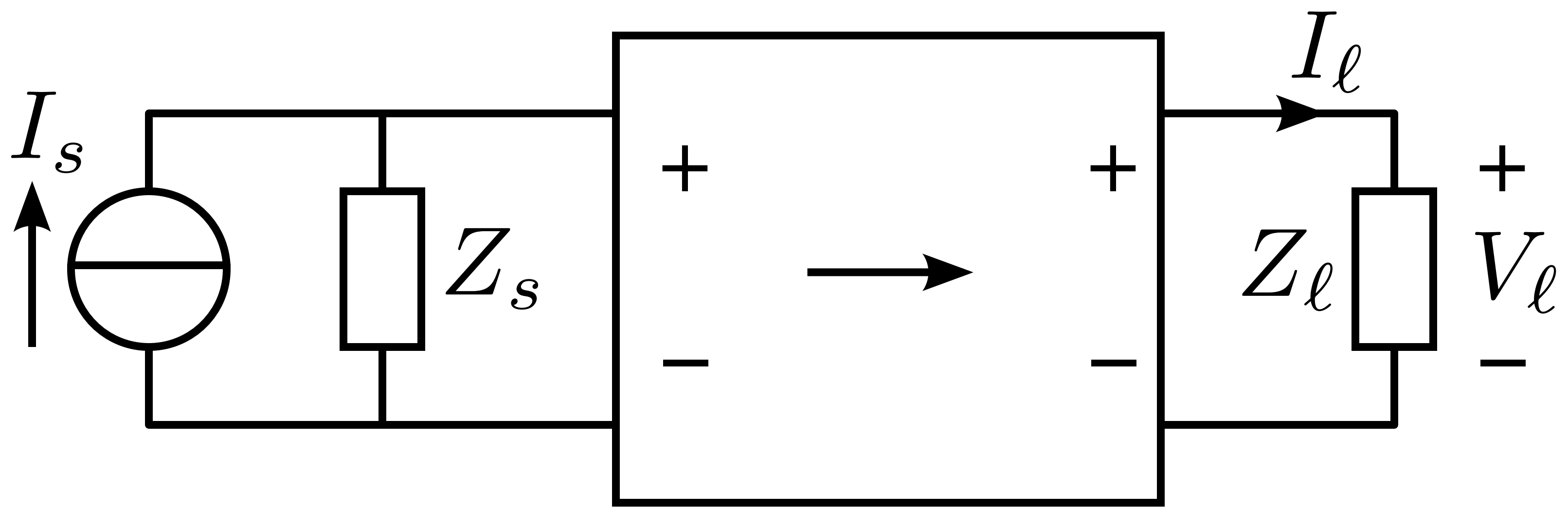


$$A_v = \frac{V_\ell}{V_s} = \frac{1}{A + B\frac{1}{Z_\ell} + CZ_s + D\frac{Z_s}{Z_\ell}}$$

$$A_y = \frac{I_\ell}{V_s} = \frac{1}{AZ_\ell + B + CZ_\ell Z_s + DZ_s}$$

Source to load transfer





$$A_v = \frac{V_\ell}{V_s} = \frac{1}{A + B\frac{1}{Z_\ell} + CZ_s + D\frac{Z_s}{Z_\ell}}$$

$$A_z = \frac{V_\ell}{I_s} = \frac{1}{A\frac{1}{Z_s} + B\frac{1}{Z_s Z_\ell} + C + D\frac{1}{Z_\ell}}$$

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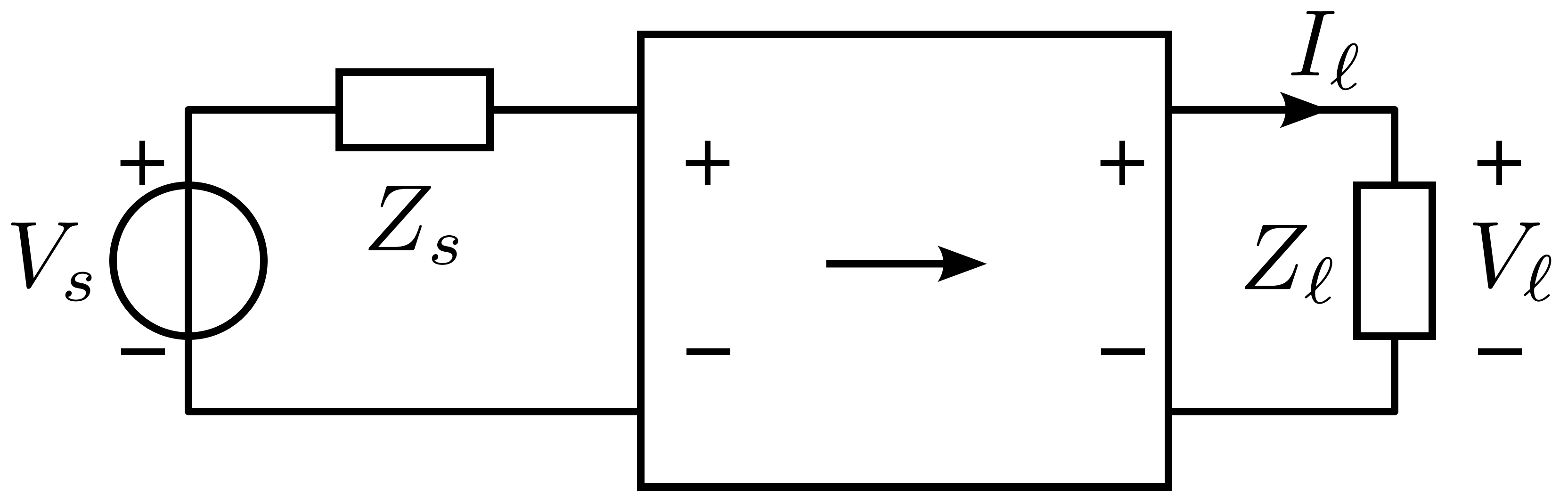

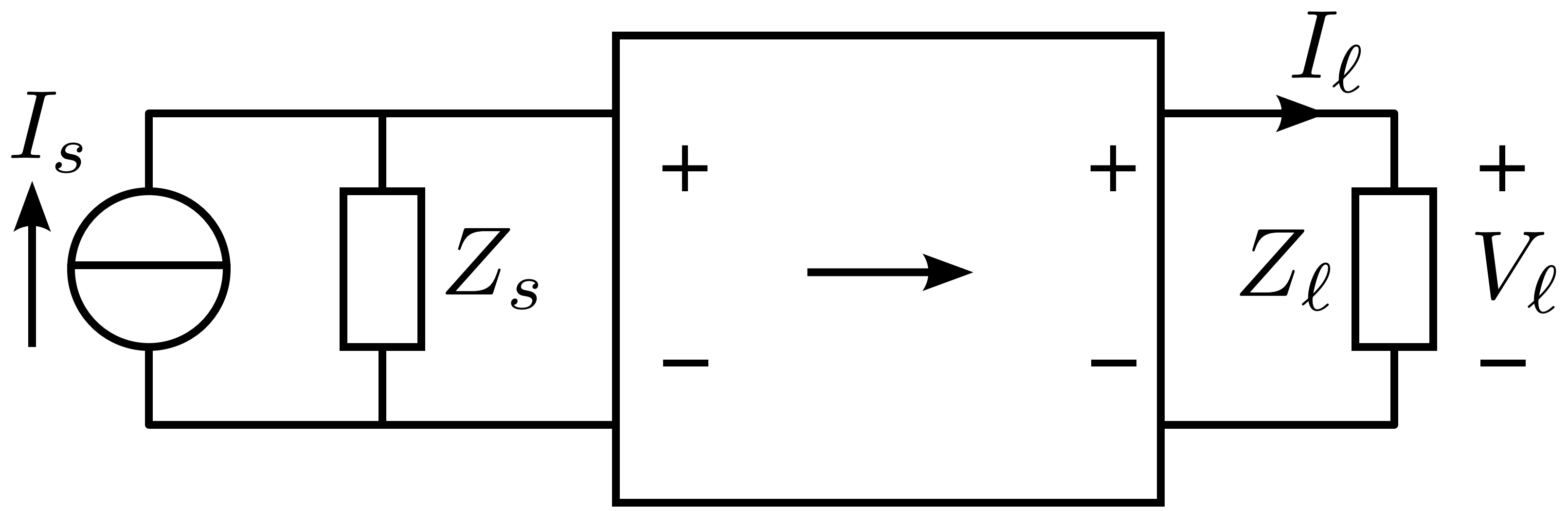

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$$A_i = \frac{I_\ell}{I_s} = \frac{1}{A\frac{Z_\ell}{Z_s} + B\frac{1}{Z_s} + C Z_\ell + D}$$

Available power gain

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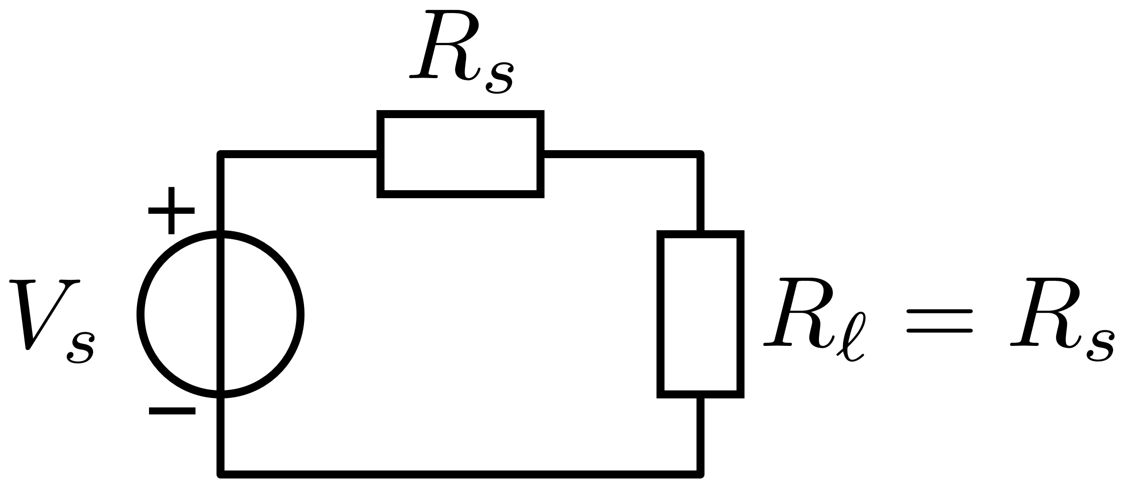
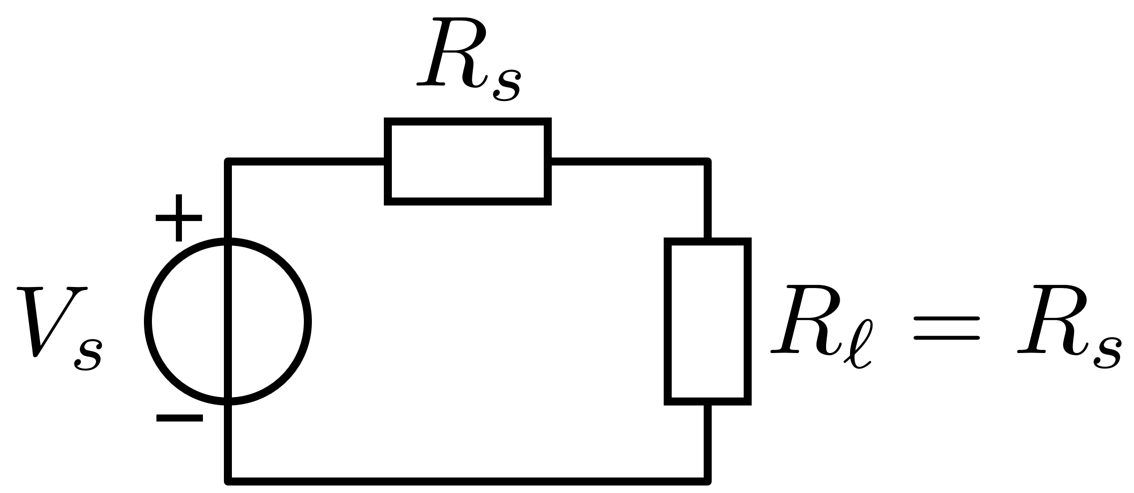


Available power of the source

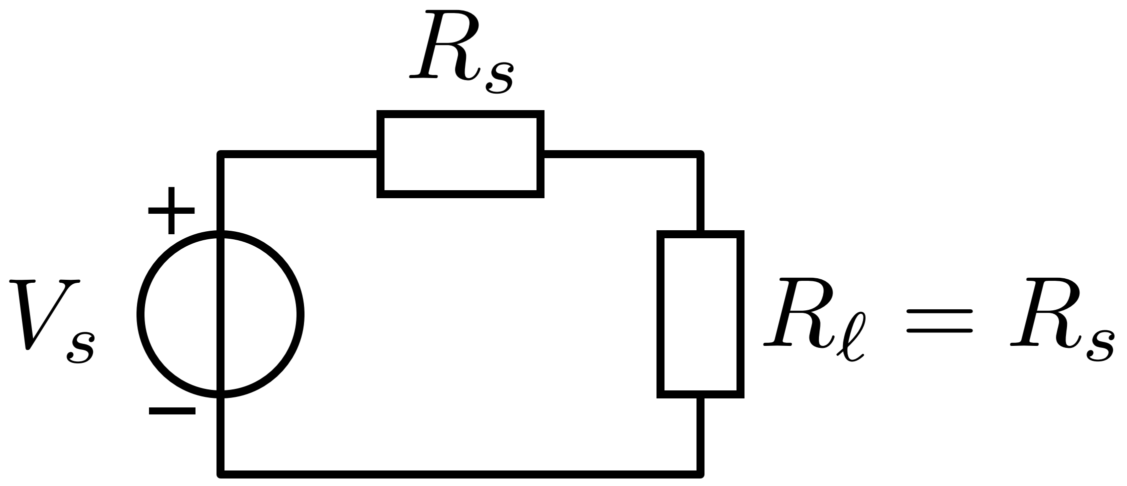
Available power gain

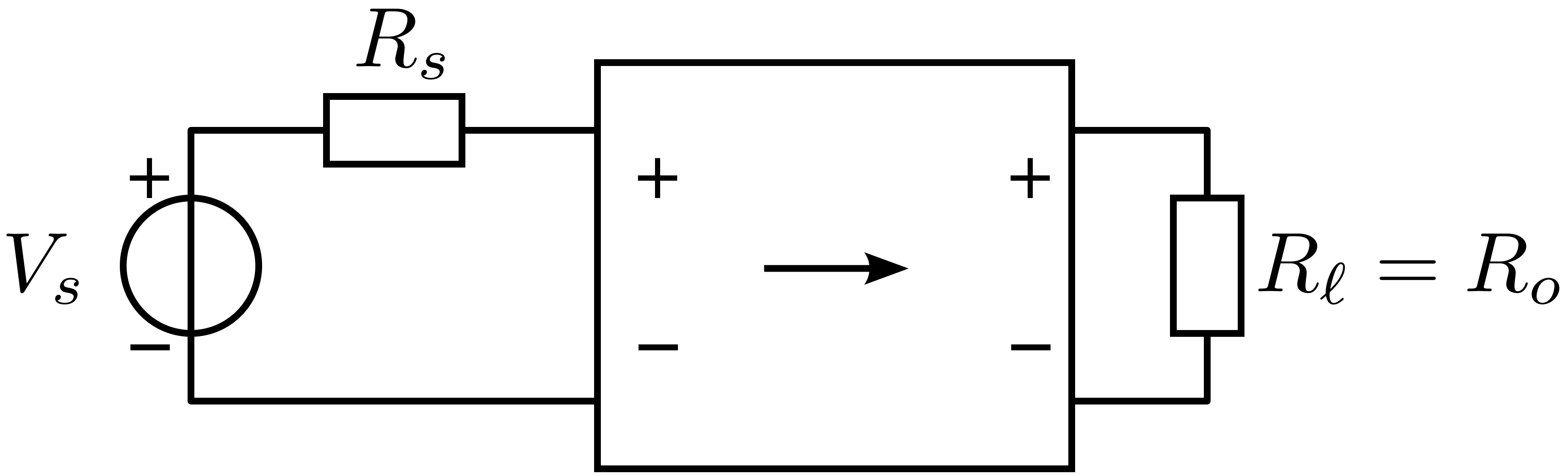


Available power of the source

$$P_s = \frac{V_s^2}{4R_s}$$

Available power gain





Available power of the source

Available power of the amplifier connected to the source

$$P_s = \frac{V_s^2}{4R_s}$$

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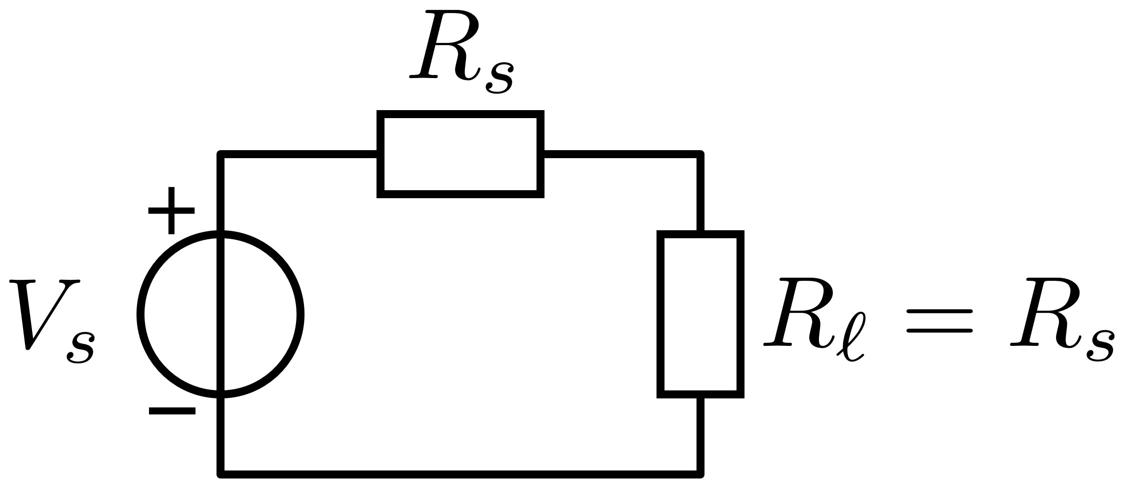
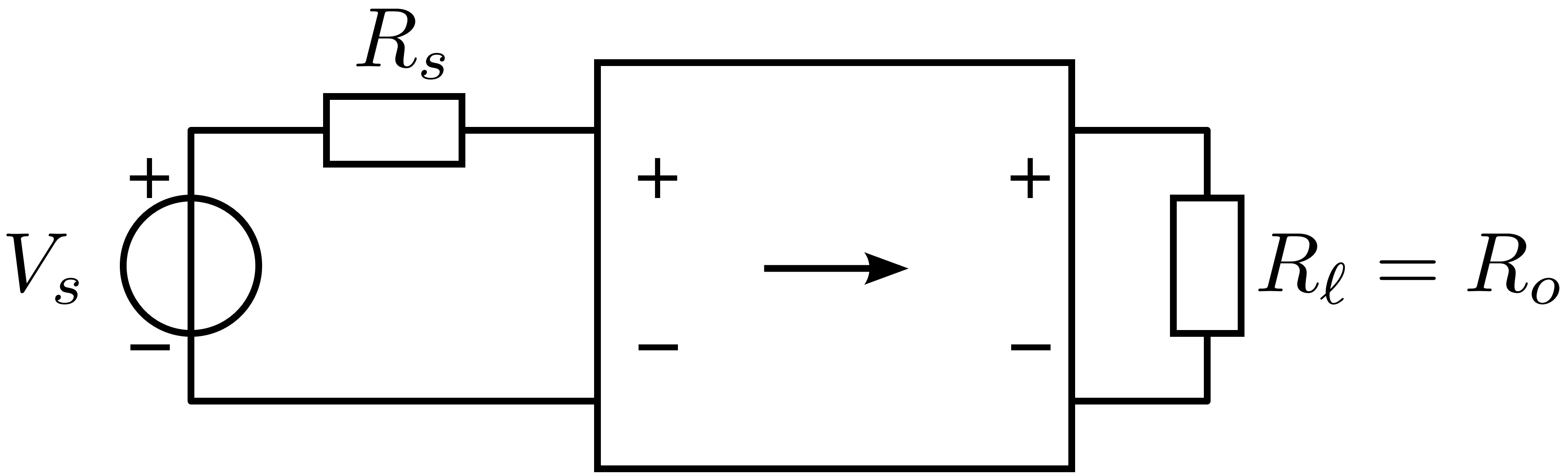




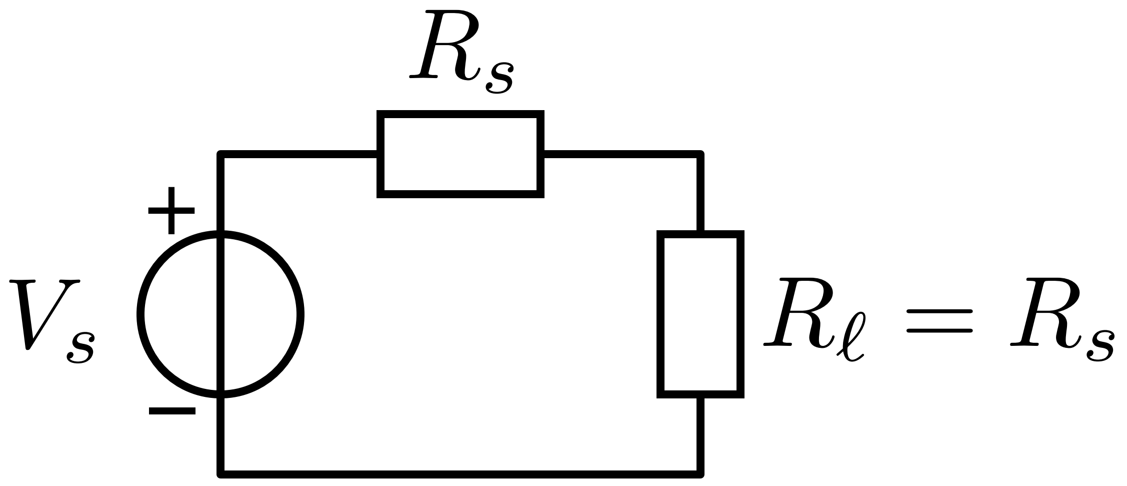
Available power of the source

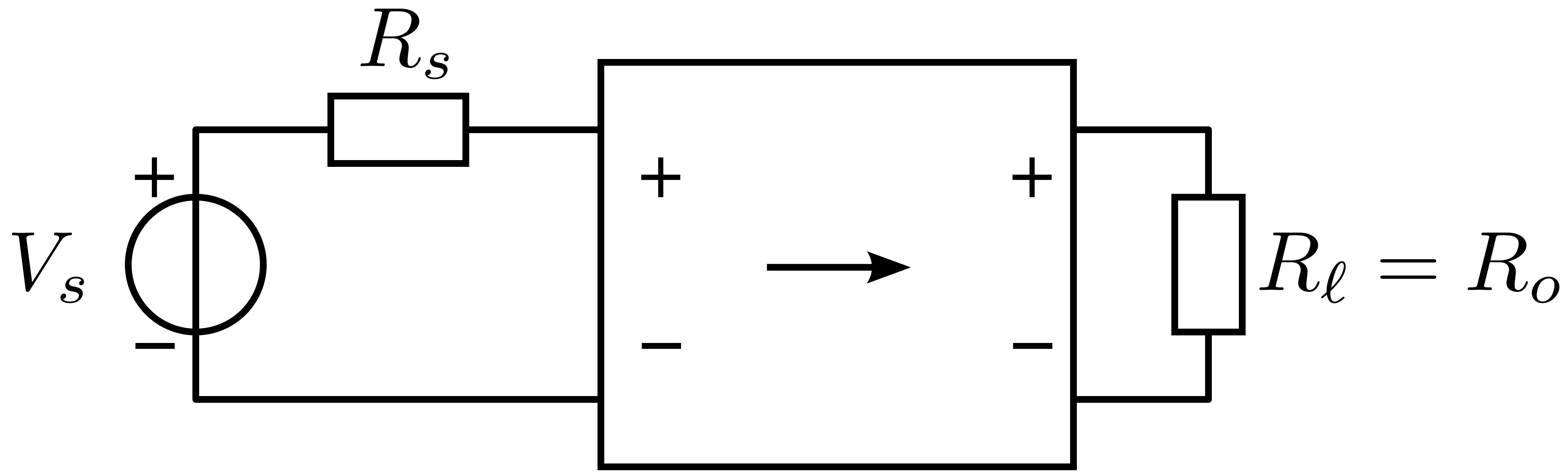
$$P_s = \frac{V_s^2}{4R_s}$$

Available power of the amplifier connected to the source

$$P_a = \frac{V_s^2}{4(DR_s+B)(CR_s+A)}$$

Available power gain





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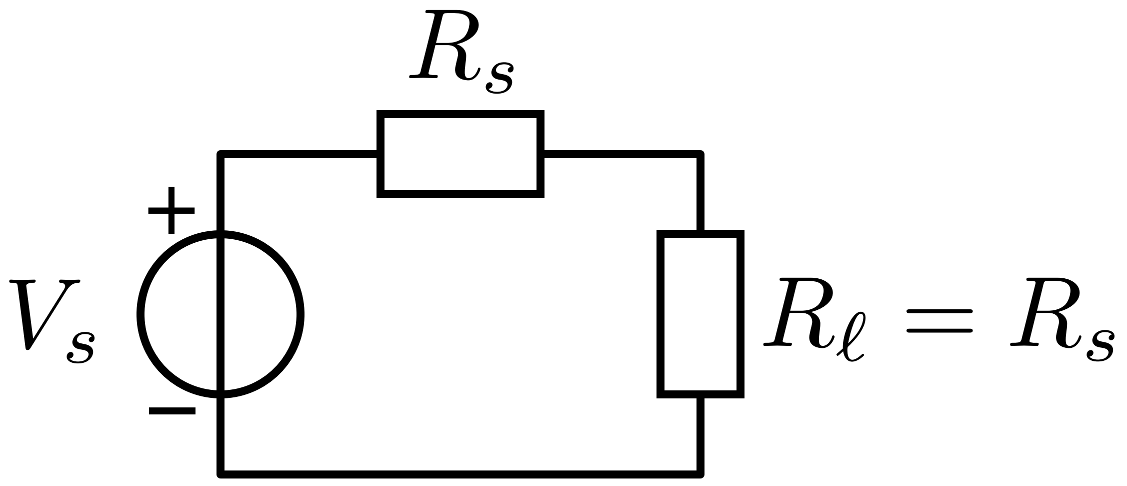

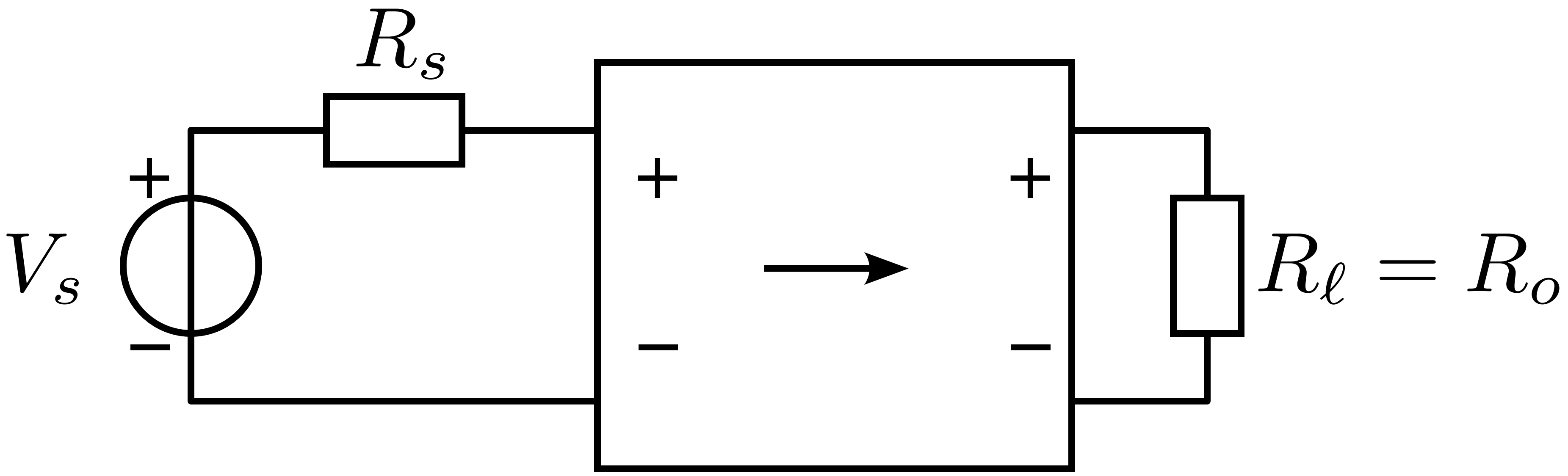

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$$G_p = \frac{P_a}{P_s} = \frac{1}{AD+AB/R_s+BC+CDR_s}$$

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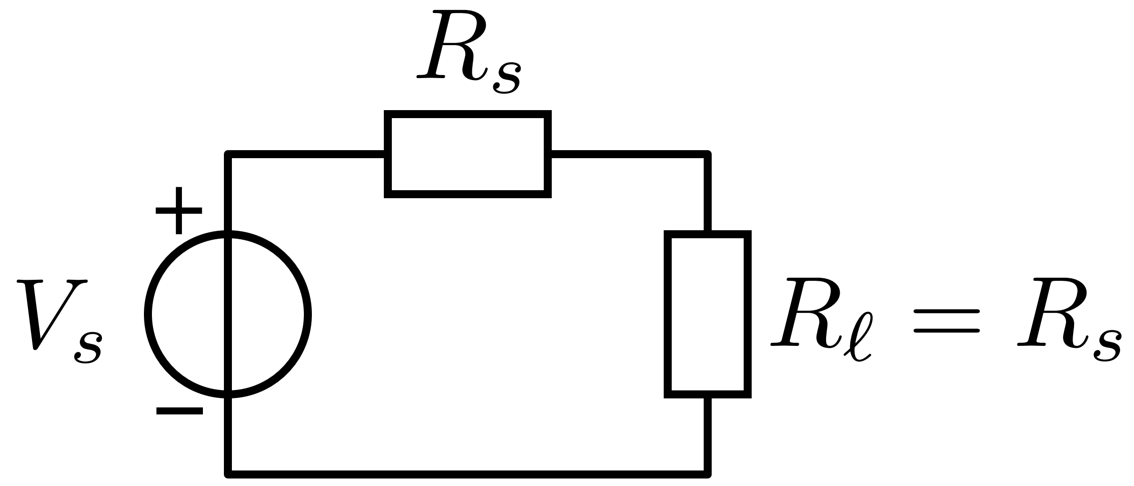

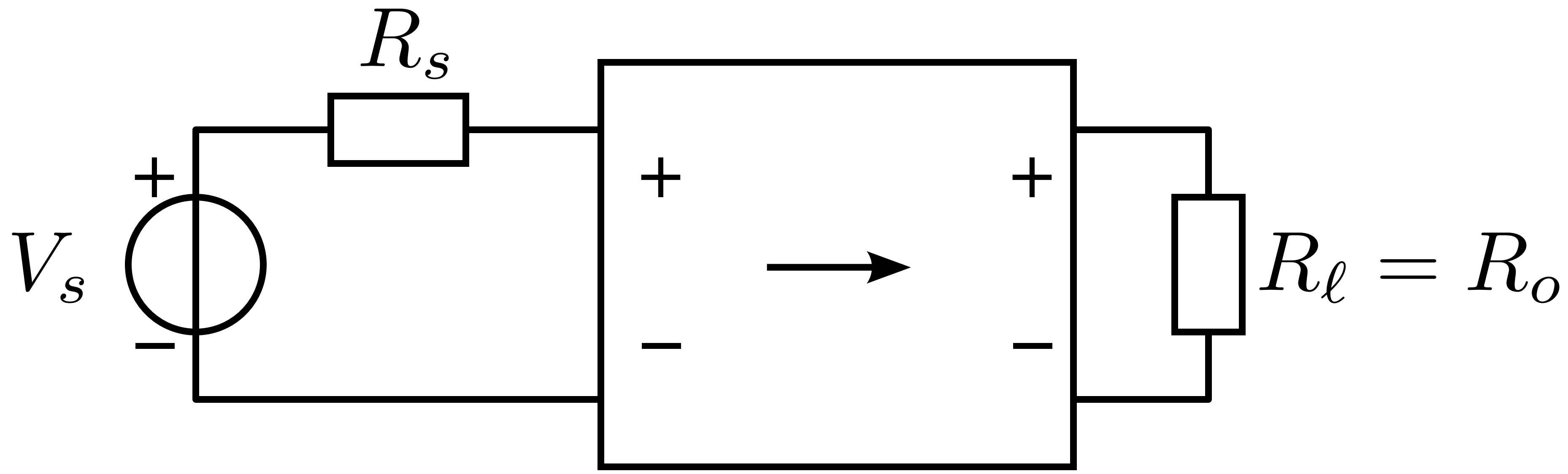

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Port impedances

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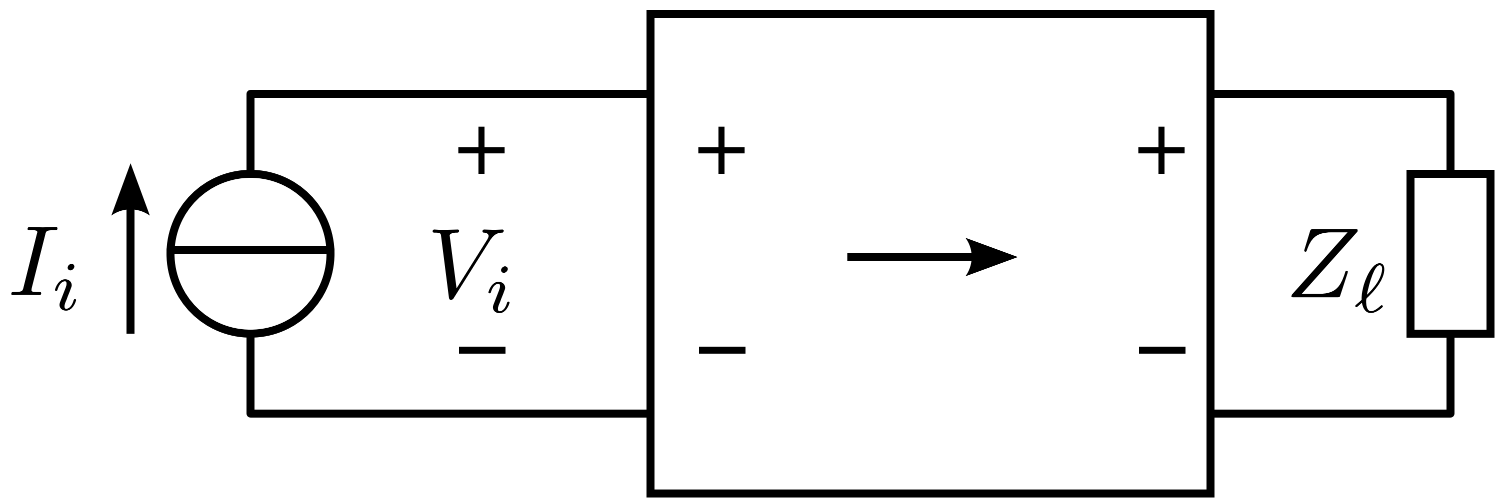
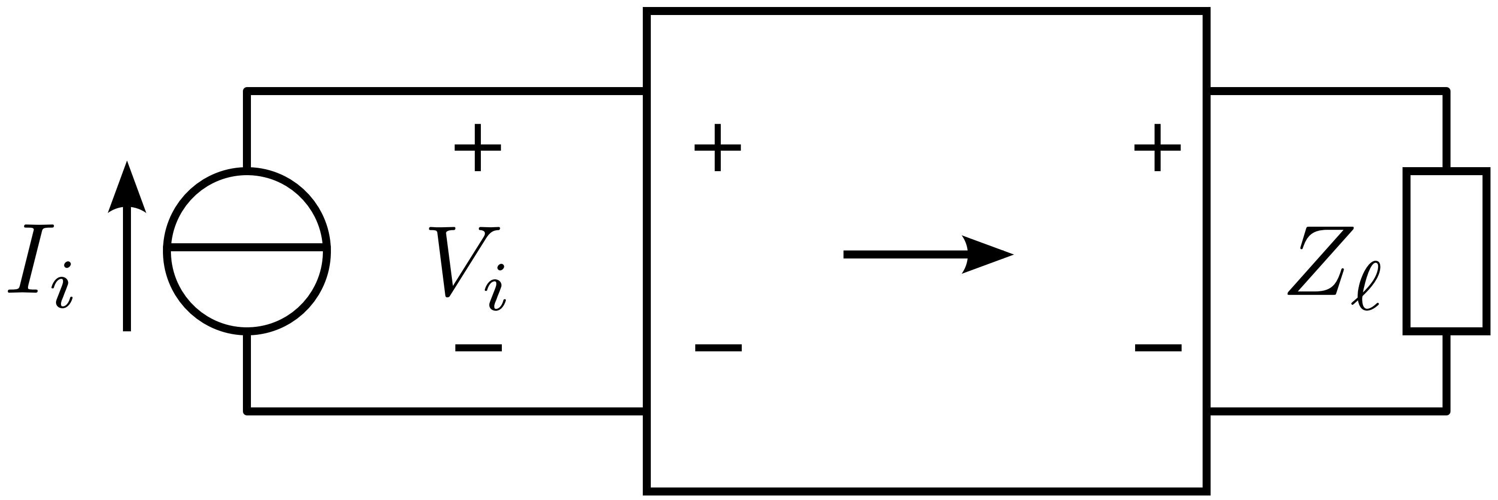
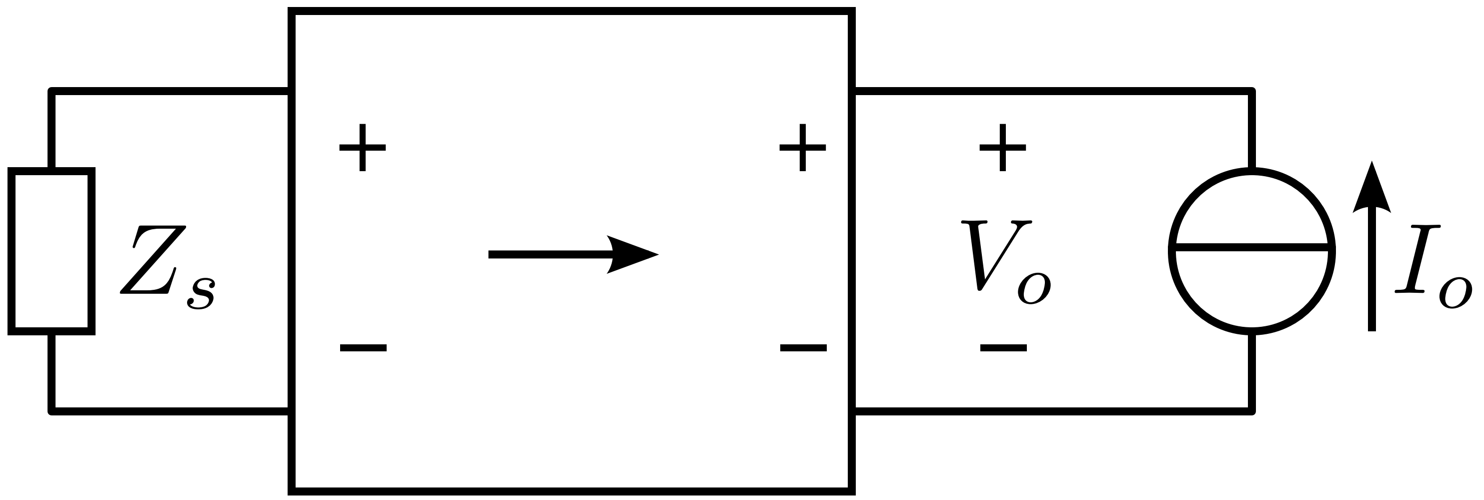


$$Z_i = \frac{V_i}{I_i} = \frac{AZ_\ell + B}{CZ_\ell + D}$$

Port impedances

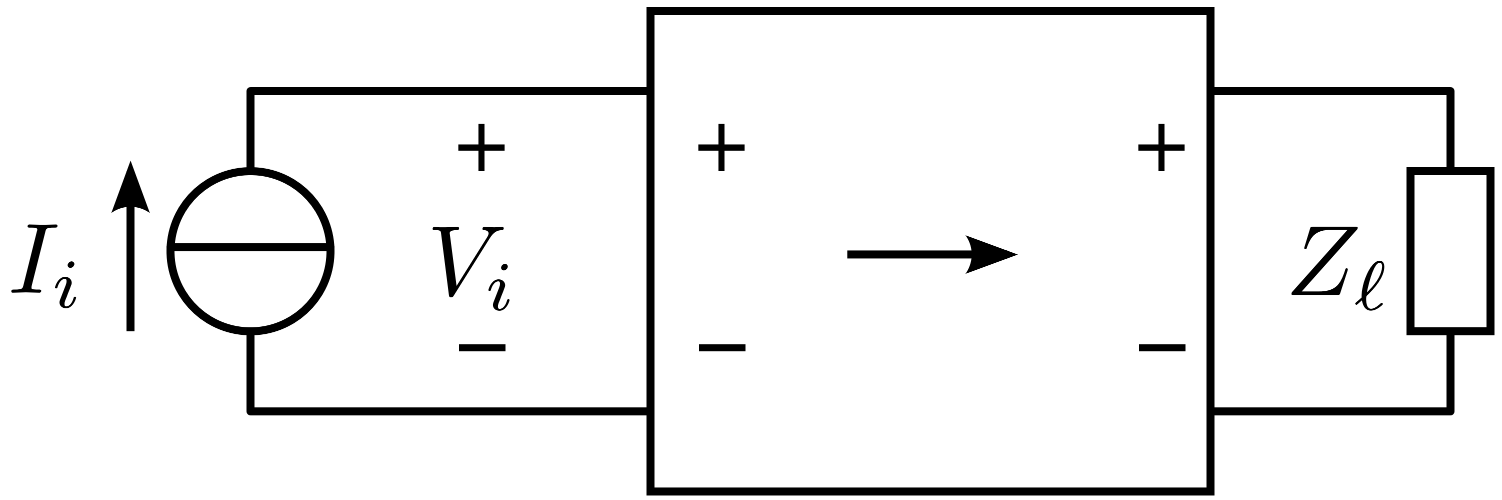


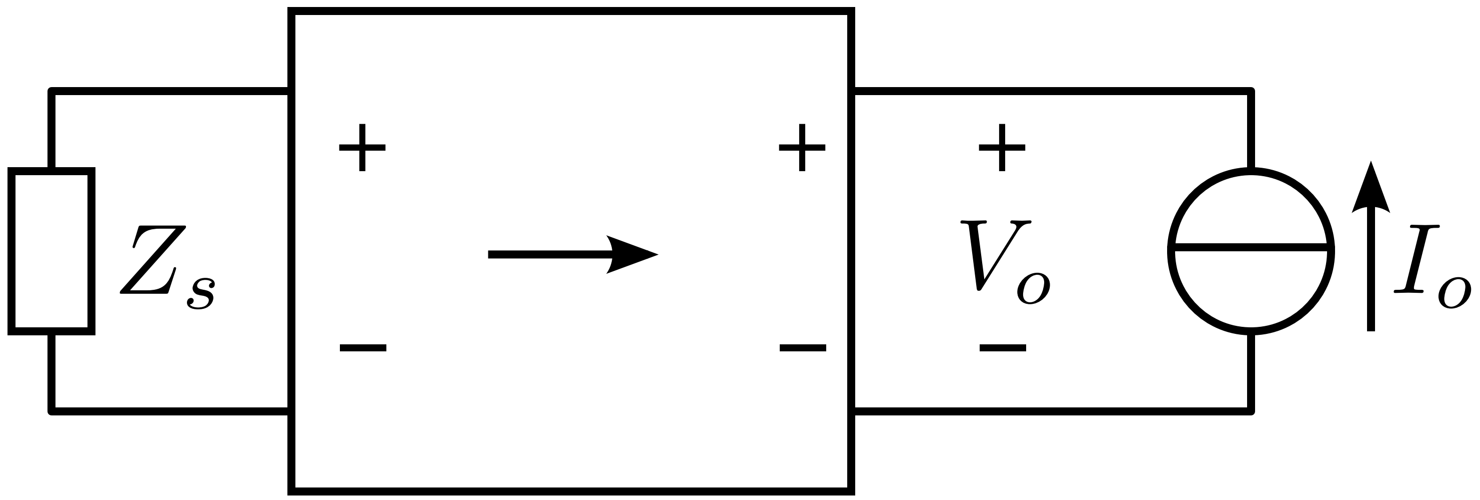


$$Z_i = \frac{V_i}{I_i} = \frac{AZ_\ell + B}{CZ_\ell + D}$$

$$Z_o = \frac{V_o}{I_o} = \frac{DZ_s + B}{CZ_s + A}$$

Port impedances





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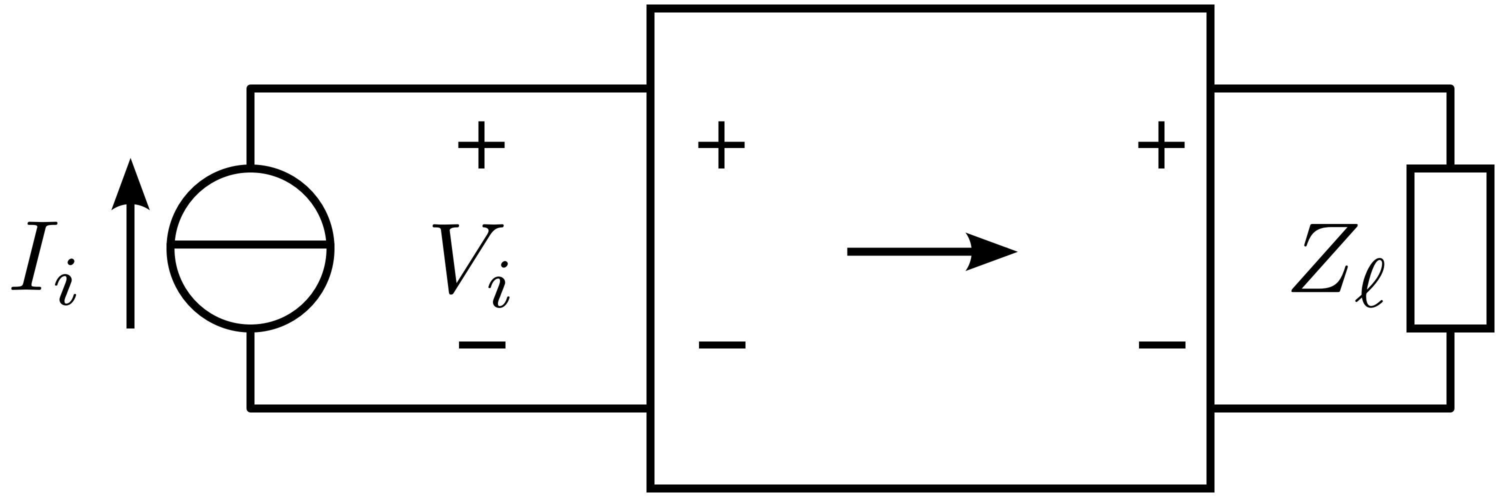
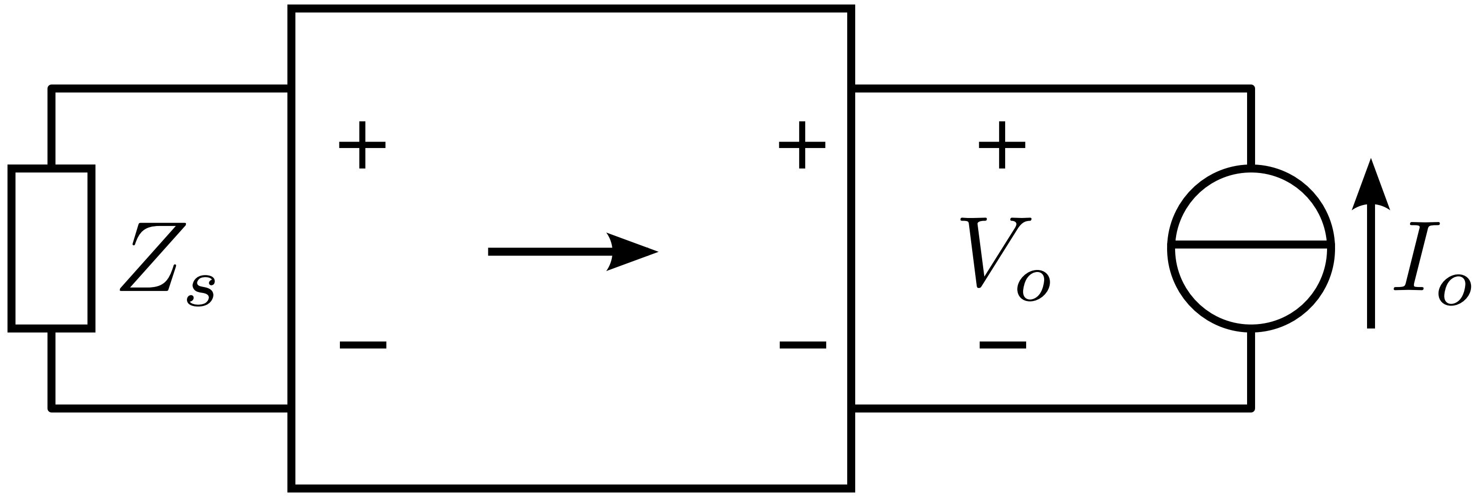
Unilateral if:

$$AD = BC$$

Port impedances





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Unilateral if:

$$AD = BC$$

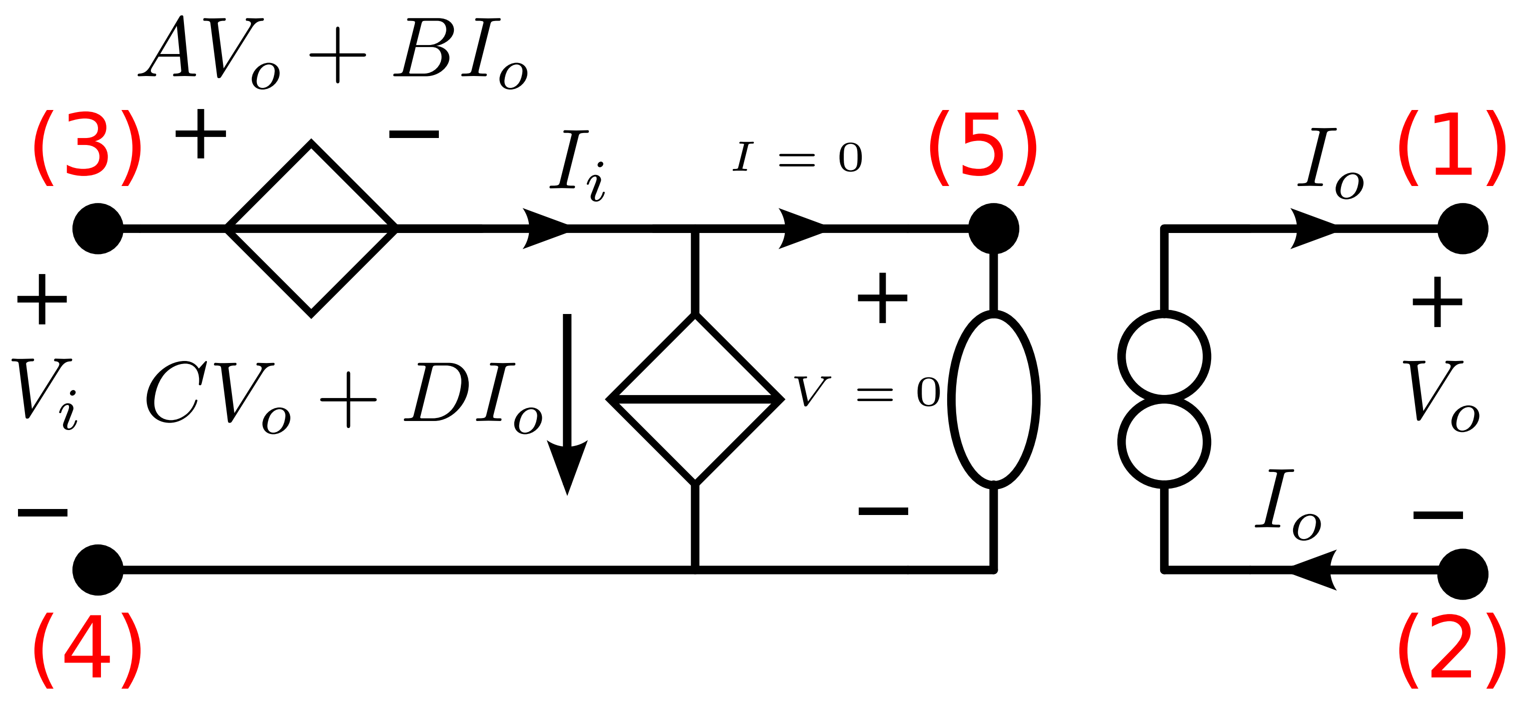
Amplifier types

Amplifier types

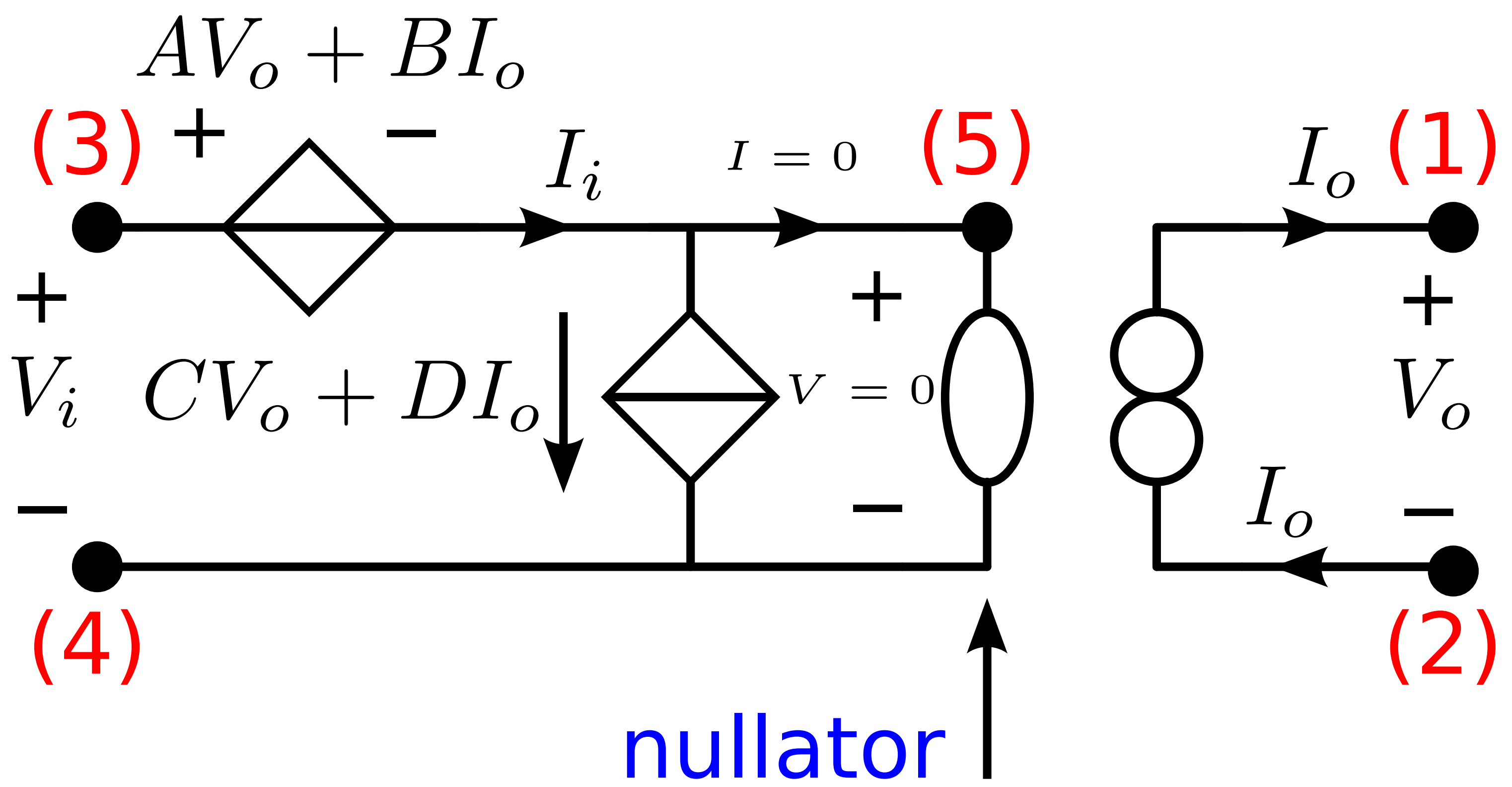
no	**amplifier type**	$\mathbf{Z}_i$	$\mathbf{Z}_o$	**A**	**B**	**C**	**D**
1	Voltage amplifier	∞	0	A	0	0	0
2	Transadmittance amplifier	∞	∞	0	B	0	0
3	Voltage input, finite nonzero output impedance	∞	Z_o	A	B	0	0
4	Transimpedance amplifier	0	0	0	0	C	0
5	Current amplifier	0	∞	0	0	0	D
6	Current input, finite nonzero output impedance	0	Z_o	0	0	C	D
7	Finite nonzero input impedance, voltage output	Z_i	0	A	0	C	0
8	Finite nonzero input impedance, current output	Z_i	∞	0	B	0	D
9	Finite nonzero input and output impedance	Z_i	Z_o	A	B	C	D

Generalized two-port model

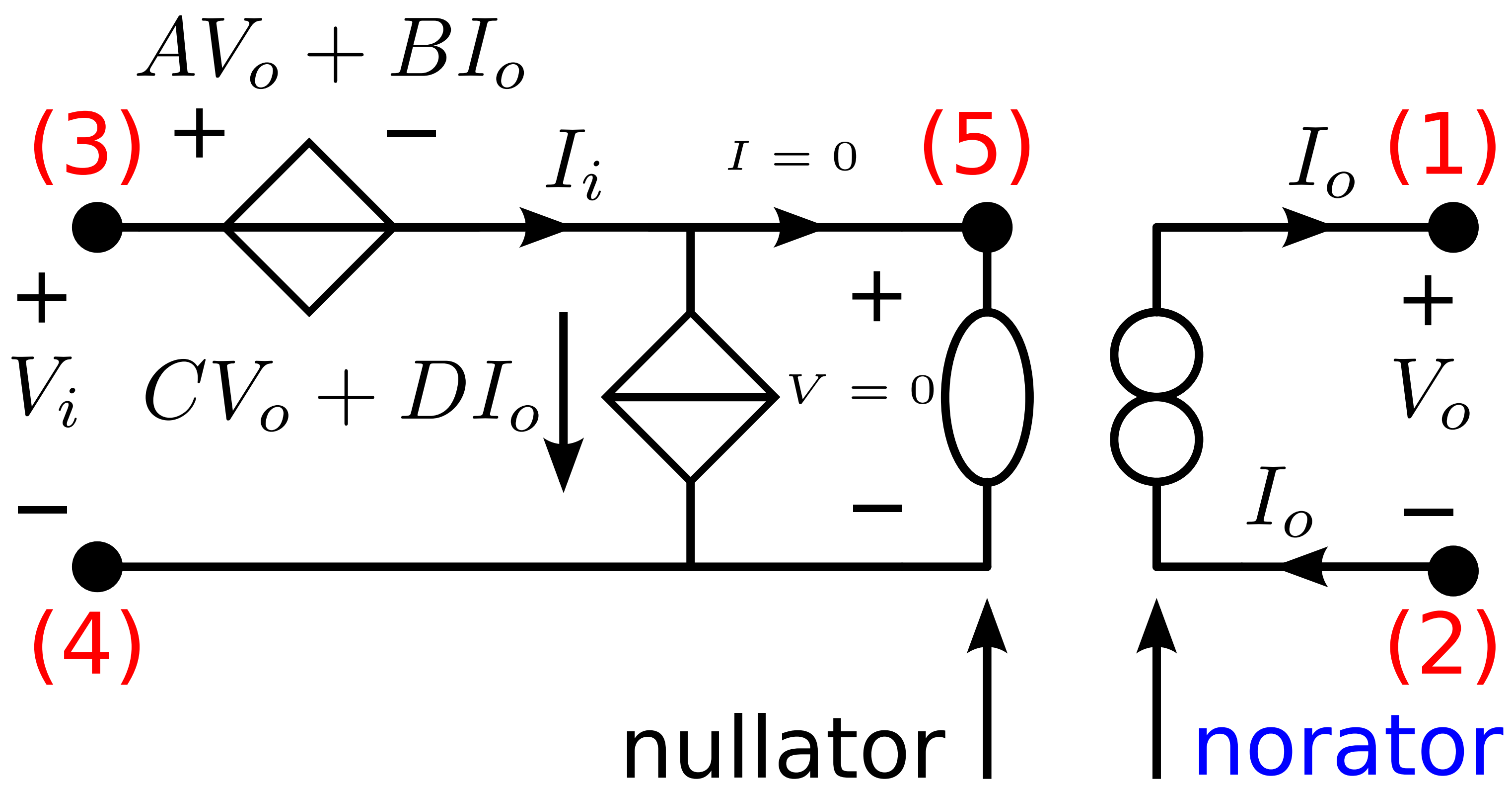
Generalized two-port model



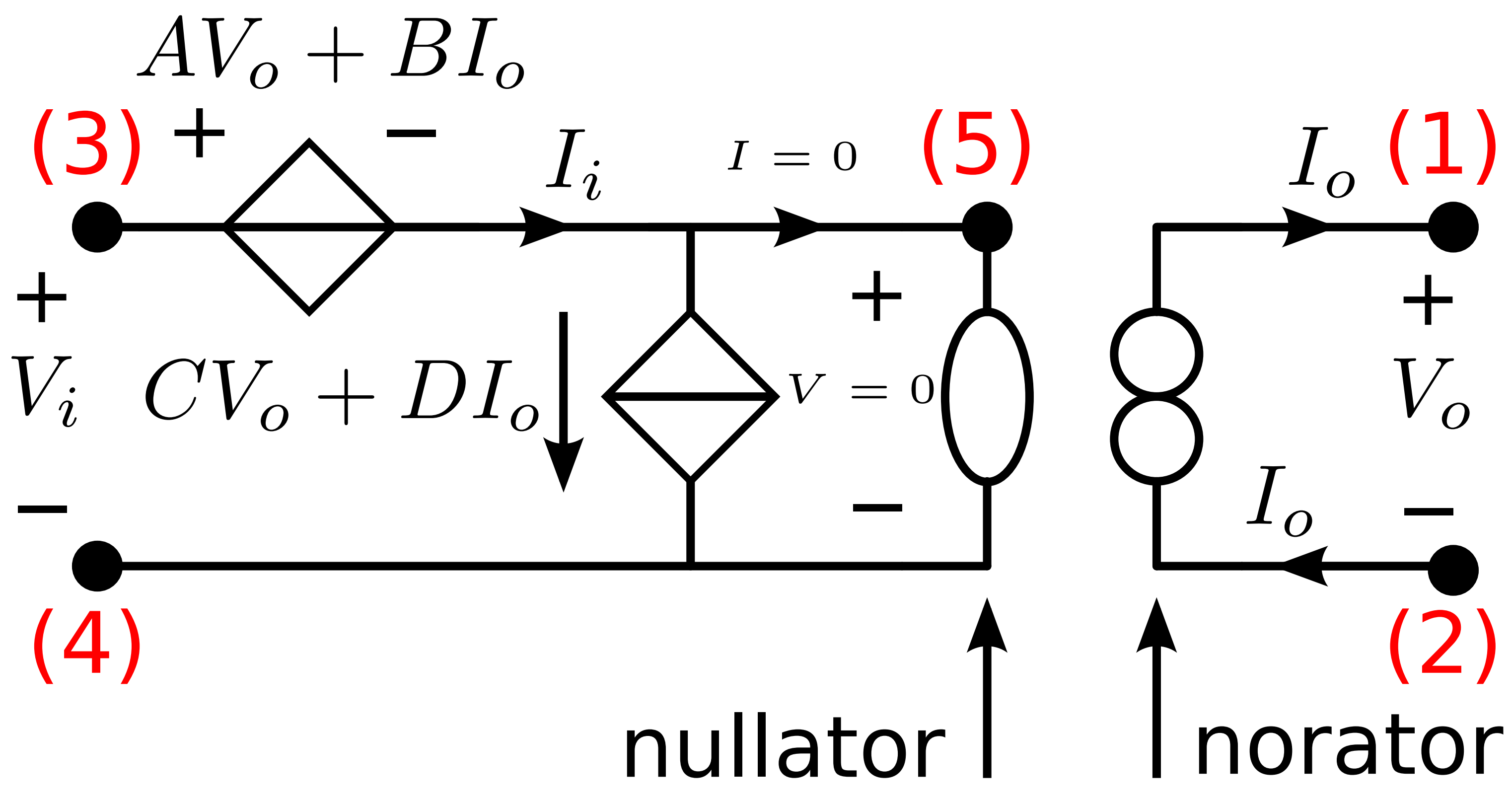
Generalized two-port model



Generalized two-port model

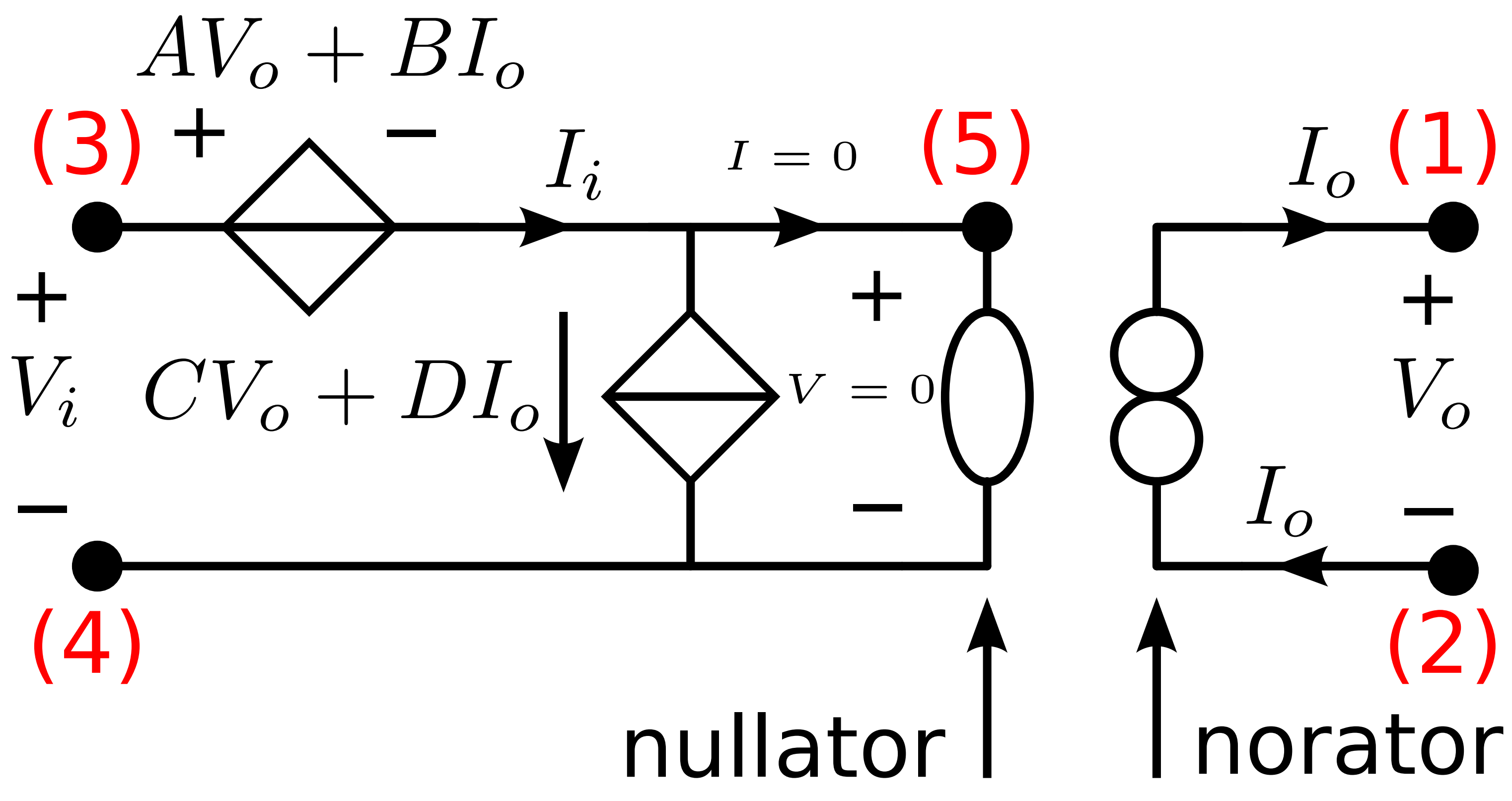


Generalized two-port model



Nullator and norator always in pairs in a network
See section 18.3.3

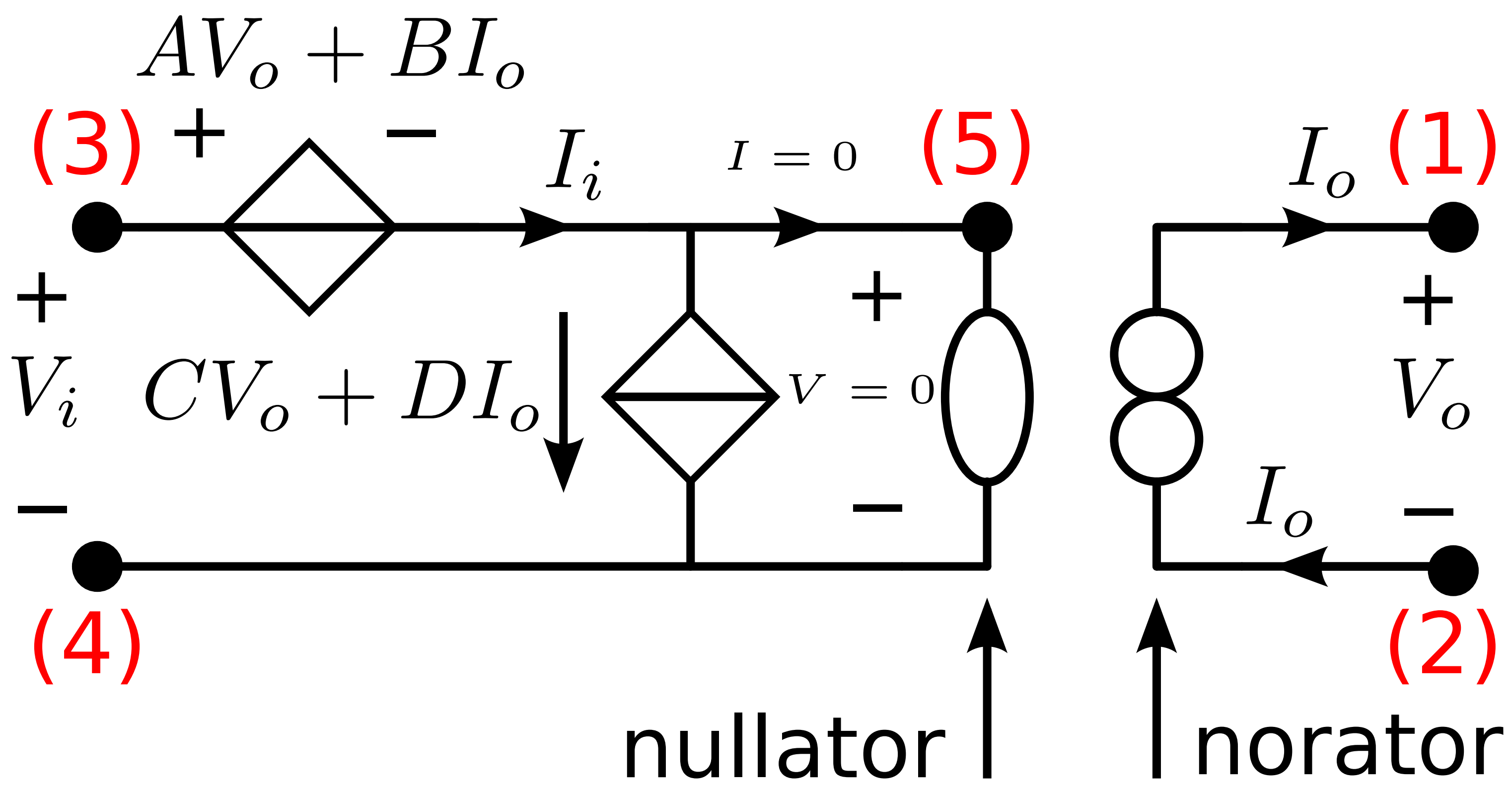
Generalized two-port model



Nullator and norator always in pairs in a network
See section 18.3.3

Nullator sets network condition

Generalized two-port model



Nullator and norator always
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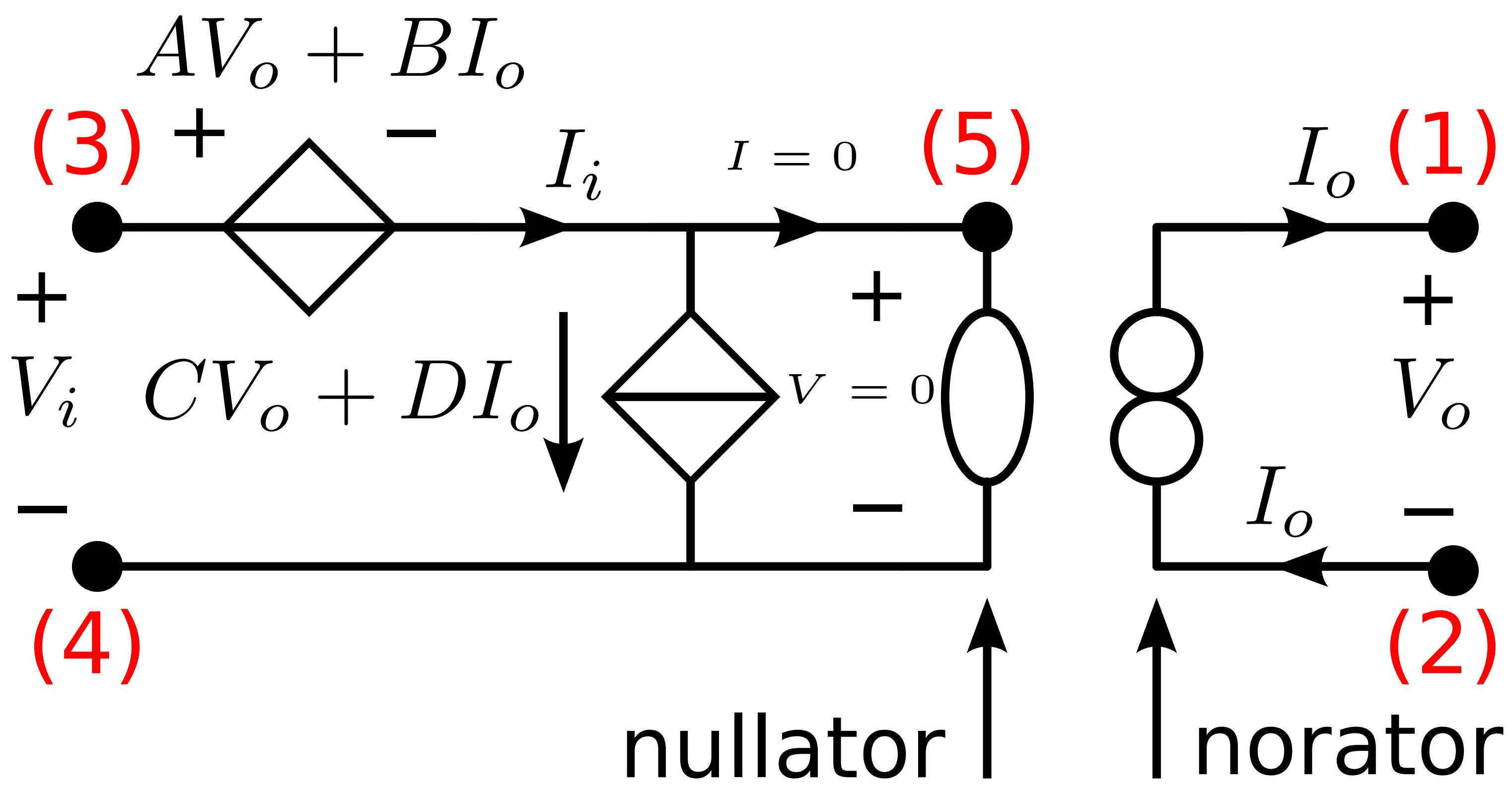
See section 18.3.3

Nullator sets network condition

Norator adds variable

Generalized two-port model



Nullator and norator always
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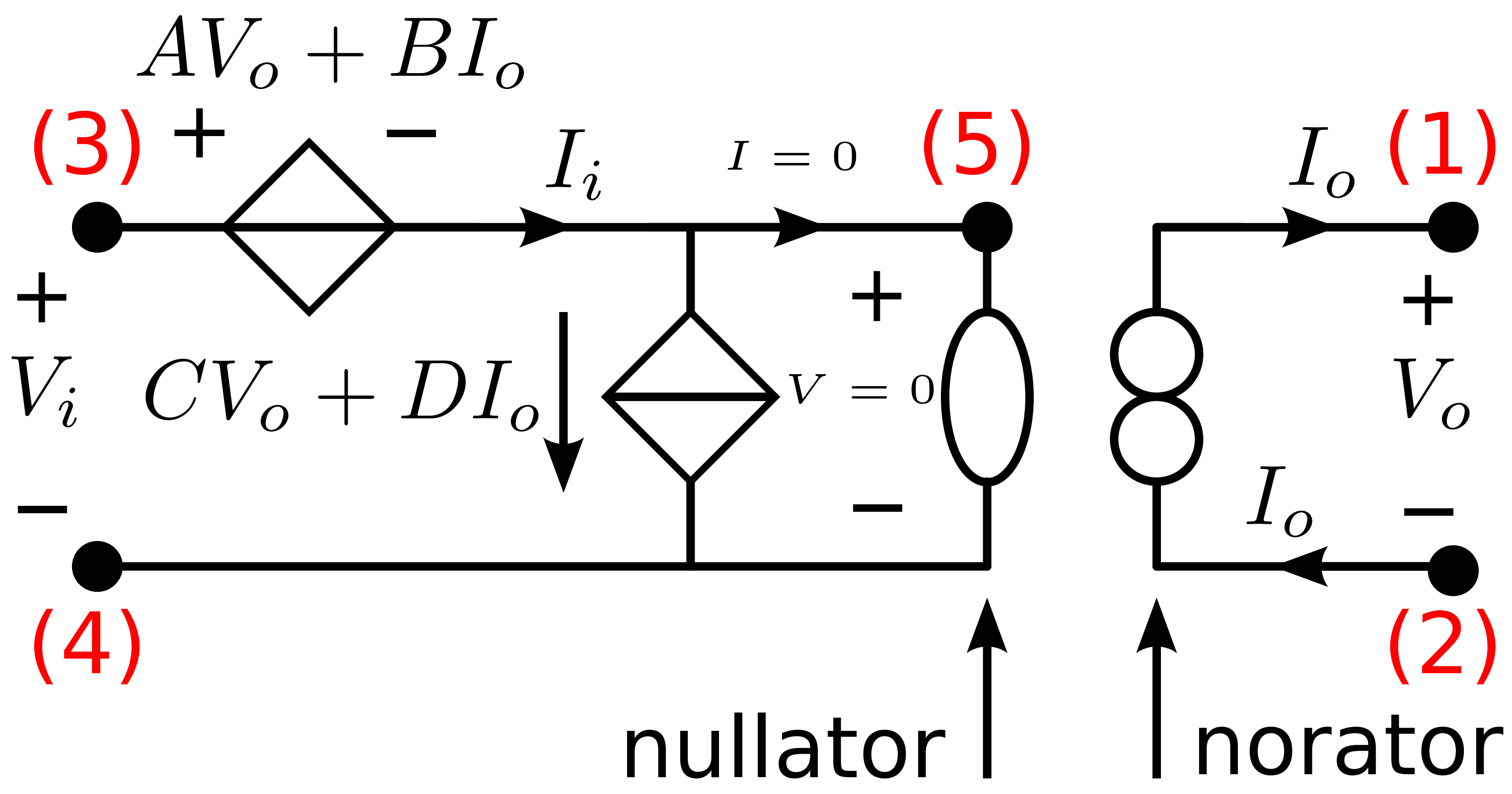
Subcircuit included in SLiCAP: symbol SLABCD in LTspice.

Generalized two-port model



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Can only be used with A,B,C,D = Real

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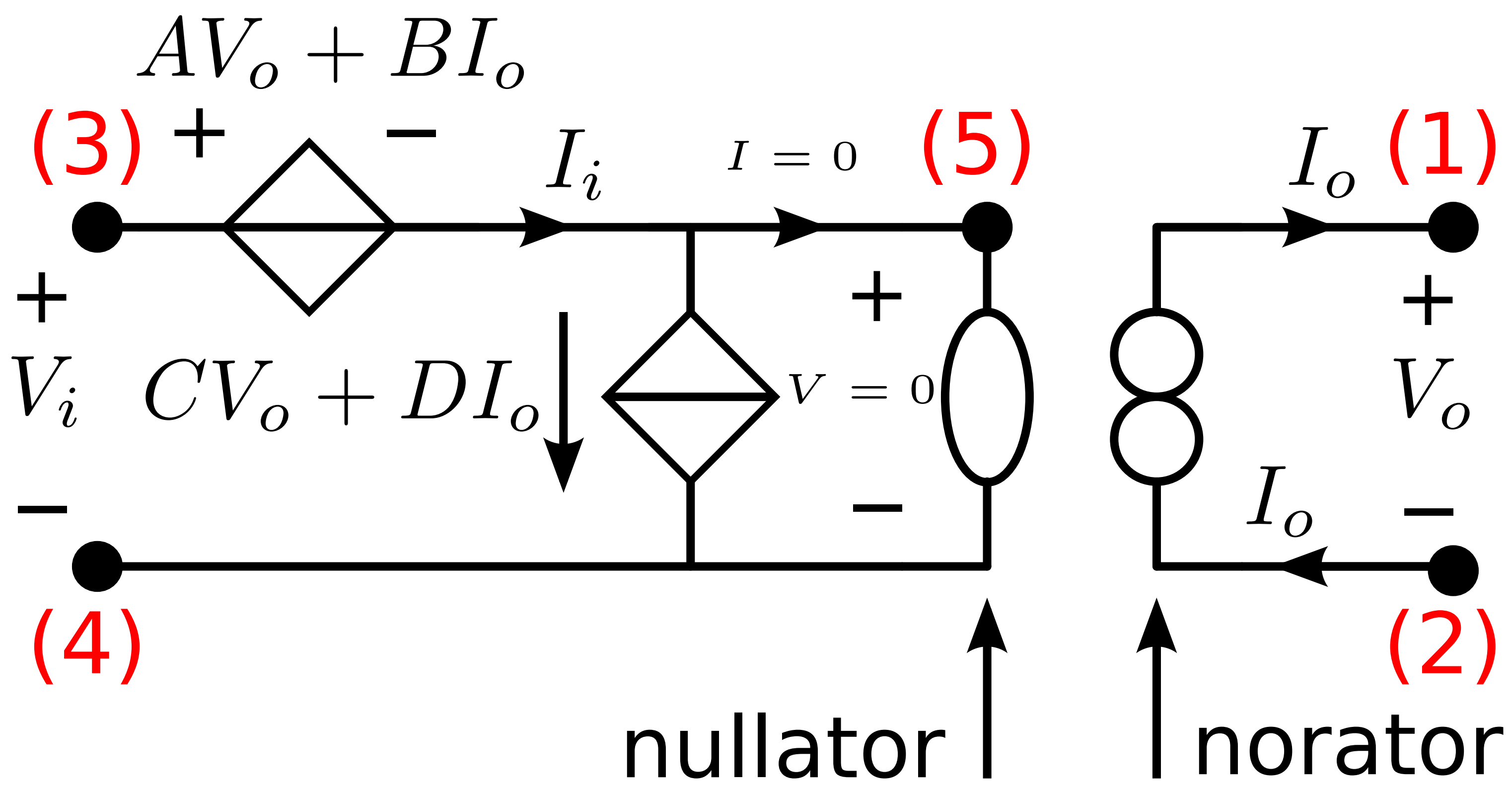

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