CMOS Controller Design

The method

From single device to multiple-stage controller

Understand basic amplification with single transistor
- The biased CS stage
- Behavior of the intrinsic CS stage (ideal drive and load conditions)
  * Static nonlinear behavior and design of voltage and current drive capability
  * Dynamic nonlinear behavior
  * Dynamic small-signal behavior
  * Noise behavior
- Behavior of the CS stage when connected between a source and a load
  * Small-signal dynamic behavior
  * Noise behavior and optimization of the noise behavior

Understand in which way the performance of a stage can be changed through application of error reduction techniques
- Application of balancing techniques: differential pair and push-pull stage
- Application of direct negative feedback: the CD and the CG stage
- Application of indirect negative feedback: the current mirror and the voltage mirror

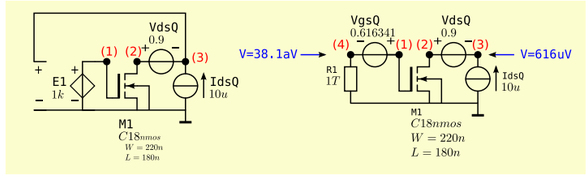
Putting it all together
- The cascode stage and the balanced cascode stage
- Controller design strategy

CS basic amplifier stage

The biased CS stage

Output port biased for performance
- Input stage: noise
- Output stage: drive capability
- Intermediate stages:
  * Drive capability
  * Contribution to:
    - LP product
    - Differential error to gain ratio

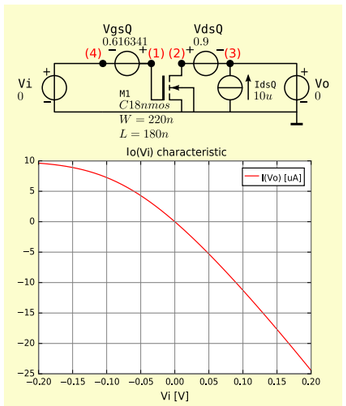
Bias sources at input port depend on device characteristics
- Can be determined by SPICE
- Biasing of particular device at simulation temperature correct for all resistive port terminations

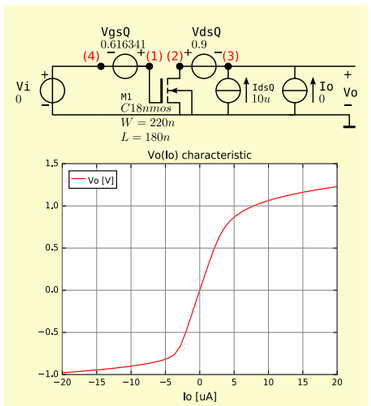


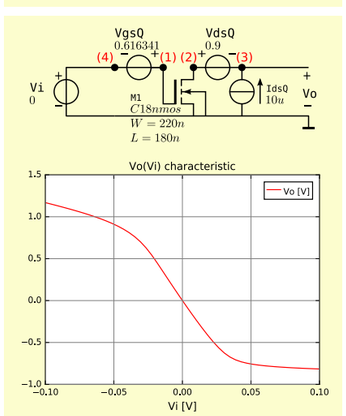
Behavior of the intrinsic CS stage

Static nonlinear behavior
- All curves pass through the origin
- Current sink capability exceeds current source capability (latter one limited by bias current)

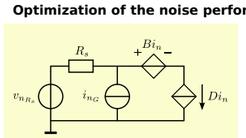
- Modeling of nonlinear effects is shown
- Other static transfers are not shown:
  * Input resistance is infinite
  * DC current gain is infinite
  * DC current to voltage transfer is infinite



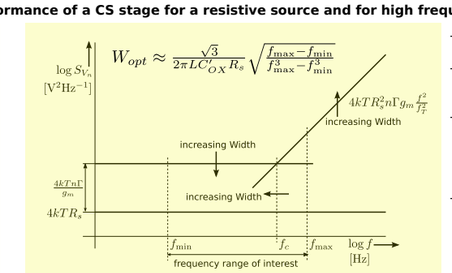




Optimization of the noise performance of a CS stage for a resistive source and for high frequencies (no 1/f noise)



$$S_{v_{n_{R_s}}} = 4kTR_s$$
$$S_{i_n} = 4kTn\Gamma g_m\left(1+\frac{f_t}{f}\right)$$
$$S_{i_{n_G}} = 2qI_G$$
$$B = -\frac{1}{g_m}$$
$$D = -\frac{sc_{iss}}{g_m} = -\frac{s}{2\pi f_T}$$

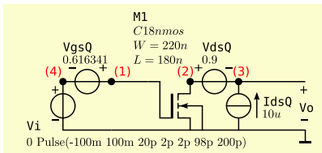


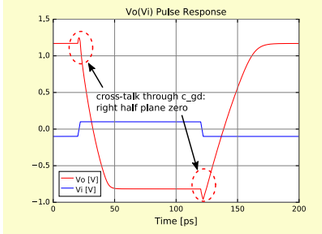
- Inversion coefficient close critical inversion
- find optimum width and best possible noise figure

- For frequencies at which the 1/f noise cannot be ignored, find optimum current and geometry through simulation.
- Lower 1/f corner frequency
  * Increase both W and L
  * Cut-off frequency will drop with square of L

$$S_{V_n} = 4kT\left(R_s+\frac{n\Gamma}{g_m}\right)\left(1+\frac{f^2}{f_c^2}\right) \qquad F_{opt} = \left(1+\frac{n\Gamma}{\sqrt{3}f_T}\sqrt{\frac{f_{max}^3-f_{min}^3}{f_{max}-f_{min}}}\right)^2$$

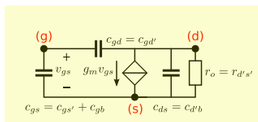
Dynamic nonlinear behavior





- Different source and sink drive capability results in different slew rate for rising and falling edges
- Right half-plane zero depend on trans-conductance and thus on the current

Dynamic small-signal behavior
Transmission-1 matrix parameters can be calculated from small-signal equivalent circuit

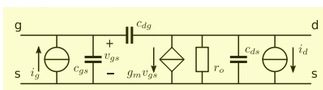


- All transfers have zero at: $s = \frac{g_m}{c_{gd}}$

  Usually above the cut off frequency

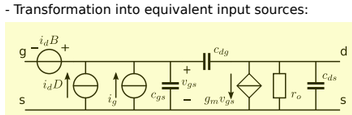
- Cut-off frequency: $\omega_T = \frac{g_m}{c_{gs}+c_{gd}}$

Noise behavior



$$S_{id} = 4kT\Gamma g_m\left(1+\frac{f_t}{f}\right)\ [A^2Hz^{-1}]$$
$$S_{ig} = 2qI_G\ [A^2Hz^{-1}]$$

- Transformation into equivalent input sources:



$$B = -\frac{1}{g_m} \qquad D = -\frac{s}{\omega_T}$$

- The noise source i_dD is called gate-induced noise. Relevant at high frequencies

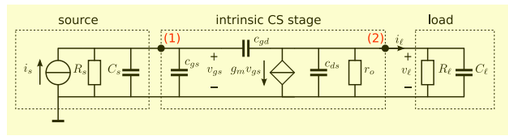
Device scaling

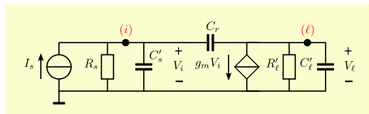
MOS Scaling parameters
- W width
- L length
- n fingers
- m devices

- Effective width: $W_{eff} = 2nmW$ source terminal always shared
  * Current-drive capability @ available V_{gs}
  * Optimization of noise performance
  * Optimization of device matching

Behavior of the CS stage between source and load

Small-signal dynamic behavior when driven/terminated from/with parallel RC





Simplified circuit

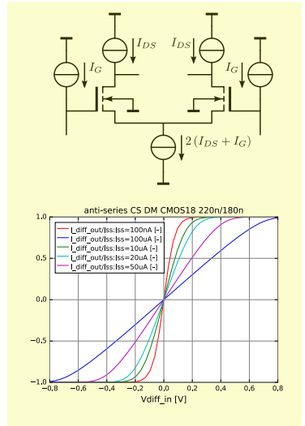
Qualitative description of the dynamic behavior (transimpedance gain)
1. If C_r=0, the circuit has two poles; associated with the two RC networks.
2. If C_r is small with respect to the other capacitances, C_r will not affect the product of the poles
   - The sum of the poles will be increased (Miller effect): one pole is closer to the origin, thus the other moves towards a higher frequency. This is called pole-splitting (due to capacitive feedback)

   - A positive zero is found at: $s = \frac{g_m}{c_{gd}}$

Pole-splitting can be used for frequency compensation.
Undesired pole-splitting may be a cause for bandwidth reduction in a feedback amplifier. This is the case if the high frequency pole is split out of the dominant group.

Balanced stages

Anti-series stage: differential pair



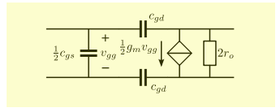
Behavioral modifications

Topology
- 4-terminal
- Behavior approximates that of natural two-port

Biasing
- Common-mode current sources only

Large signal static behavior
- Even terms cancel
- Limiting current characteristic

Small-signal dynamic
- Transmission coefficients A and D equal those of consituting elements
- Coefficient B twice as large
- Coefficient C half



Noise Behavior
- Voltage noise spectrum twice as large
- Current noise spectrum half that of individual transistors

Complementary parallel stage: push-pull stage

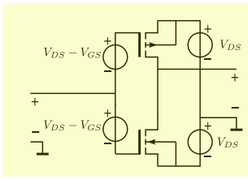
Topology
- Can be used as 4-terminal with split-signal output, but not a natural two-port

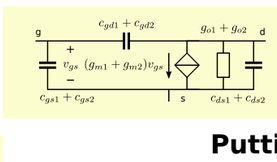
Biasing
- Common-mode voltage sources only

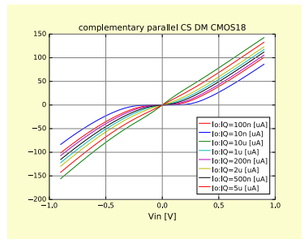
Large signal static behavior
- Even terms cancel
- Expanding current characteristic
- Imperfect balancing PMOS and NMOS

Small-signal dynamic
- Transmission coefficients A and D equal those of consituting elements
- Coefficient B half
- Coefficient C twice as large

Noise Behavior
- Voltage noise spectrum half that of constituting transistors
- Current noise spectrum twice as large

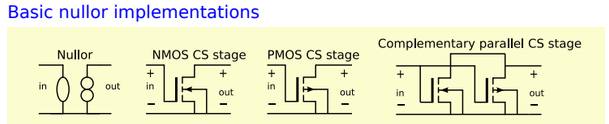


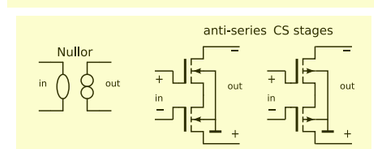




Local feedback stages

Basic nullor implementations

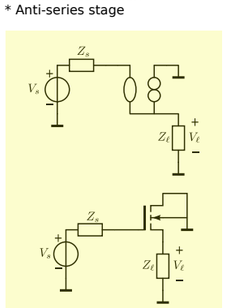




Local feedback stages
- Feedback with a basic amplifier stage as controller
- 3 terminal controller:
  * CS stage
  * Complementary-parallel stage
- 4-terminal controller:
  * Anti-series stage

The CD stage or source follower

Non-energic feedback unity-gain voltage amplifier
- Behavioral modifications through application of negative feedback:
  * Nonenergic: equivalent input noise sources equal those of its CS stage controller
  * Parallel voltage sensing: decreases output impedance
  * Series voltage comparison: increases input impedance
- Feedback not effective if sensing or comparison not possible:
  * Output shorted
  * Input current-driven
- Back-gate effect reduces loop gain
- Poles may be complex with capacitive load



Putting it all together

Input stage

CS, CE, balanced version, preferably cascode
- Best possible nullor approximation
- Best possible contribution to LP product and DG ratio
- Determine device geometry range and operating current range that satisfies noise requirements
  * Model the controller as a nullor with the noise sources of the input device, with geometry and operating current as design parameters

Output stage

CS, CE, balanced version, preferably cascode
- Best possible nullor approximation
- Best possible contribution to LP product and DG ratio
- Use complementary-parallel stage for improved power efficiency
- Determine device geometry range and operating current range that satisfies the drive requirements
- Also determine the drive conditions for this stage

Intermediate stages

CS, CE, balanced version, preferably cascode
- Best possible nullor approximation
- Best possible contribution to LP product and DG ratio

Number of stages

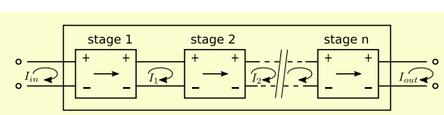
Single stage controller
- If device geometry and operating requirements for input and output stage overlap

Two-stage controller
- If the drive requirements for the output stage overlap with the operating conditions for the input stage
- If the LP product of the loop gain of this two-stage solution satisfies the bandwidth requirements
- If the differential error to gain ratio of this two-stage solution satisfies the distortion requirements

Multiple-stage controller
- If conditions for a two-stage controller are not satisfied
- Consider application of passive local feedback stages:
  * Increase loop gain without adding a dominant pole

Interconnection of stages

Maintain two-port conditions for the controller



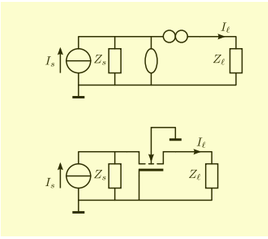
Biasing

Method: maintain DC coupling between stages
- Redirect bias current sources via the power supply
- Minimize the number of floating voltage sources (level shifts)
- Apply error reduction techniques for improvement of
  * Common-mode biasing
    - Common-mode feedback
  * Biasing of stages
    - Model-based feedback (indirect feedback)
  * Reduction of over-all operating point drift and in accuracy
    - AC coupling
    - AC coupling + over-all biasing feedback

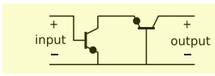
General: maintain two-port conditions for the controller
- Avoid signal current flowing to the power supply or ground
- Ensure a low impedance for supply voltages and minimize supply noise, particularly in cases in which both the ground and the supply node are used as signal reference

The CG stage

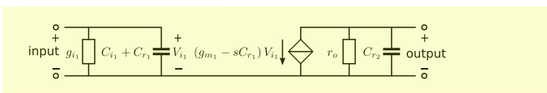
Non-energic feedback unity-gain current amplifier
- Behavioral modifications through application of negative feedback:
  * Nonenergic: equivalent input noise sources equal those of CS stage
  * Series current sensing: increases output impedance
  * Parallel current comparison: decreases input impedance
- Feedback not effective if sensing or comparison not possible:
  * Output left open
  * Input voltage-driven
- Back-gate effect increases loop gain
- In practice a large loop gain if driven from and terminated with a CS stage



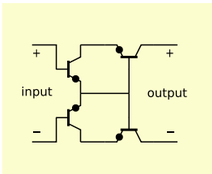
Cascode stages



CS-CG or CE-CB cascade = cascode stage
- Elimination of pole-splitting (shorted CS or CE stage)
- Approximate unilateral behavior
- High output impedance
- Non dominant pole of CG or CB stage at f_T
- Almost ideal CS or CE stage



Balanced cascode stage



- Best possible single-stage nullor implementation
- Best possible single-stage natural two-port approximation
- Approximate unilateral behavior
- High output impedance
- Non dominant pole of balanced CG or CB stage at f_T