Device modeling

Modeling of 'Active Devices'

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Introduction

Aim of this lecture

1. Understand the basic operation of amplifying devices
   - MOSFETs
   - BJTs
   - JFETs
2. Be able to model performance aspects relevant for amplifier design
   - Static behavior
   - Dynamic behavior
   - Noise behavior
   - Operating regions

Introduction

Analysis types and device models

1. Symbolic analysis for setting up design equations
   - Parameterized small-signal models
     - Behavior linearized in operating point
   - Model parameters depend on
     - Device type and characteristic
     - Device geometry
     - Operating point
2. Numeric analysis for design verification
   - Static behavior (DC analysis model)
   - Small-signal dynamic behavior (AC analysis model)
   - Large signal dynamic behavior (Transient analysis model)
   - Small-signal dynamic noise behavior (Noise model)

Introduction

All models are wrong

- Simulators give high-resolution output (many digits)
- Predictability of the circuit behavior can still be low:
  - Have the relevant physical effects been modeled (accurately)?
  - Have the model parameters been extracted from the measurement data (correctly)?
  - Have the correct numeric algorithms been implemented (accurately)
  - Have statistical deviations been described (correctly)?

MOS transistors

Technology

- Field effect devices with their gate isolated from the channel by SiO_2
  - The Metal Oxide Semiconductor Transistor was invented by Kahng and Dawon in 1959
  - The first CMOS circuit has been reported in 1963 by Wanlass and Sah
  - Aluminium and polysilicon are commonly used as gate materials
- Depending on their application MOS transistors are fabricated in different ways:
  - Standard IC CMOS lateral devices with a symmetrical structure
  - Modern IC Fin FETs with a three dimensional gate structure
  - Lateral or vertical high-voltage MOS transistors of which the low-voltage gate-source structure differs from the high-voltage gate-drain structure

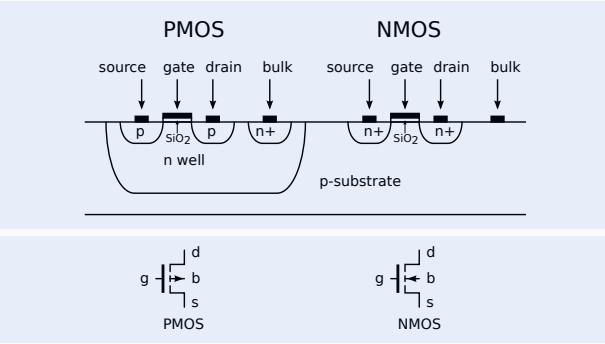
MOS transistors

Application

- MOS transistors found their first application in digital circuits
- High-volume analog ICs and mixed signal ICs nowadays predominantly fabricated in CMOS technology
- Power MOS transistors are available in high-voltage IC processes and as discrete devices, mostly used as power switches in switched regulators and switched amplifiers

MOS transistors

Structure



MOS transistors

Operation: weak inversion

- Assume:
  - Source and the bulk (substrate) of an NMOS have been connected to a reference potential (0V)
  - Drain has been connected to a fairly large positive voltage V_{DS}.
- Brief description of $I_{DS}(V_{GS})$ in weak inversion
  - $V_{GS} = 0$: bulk *surface potential* Ψ_s defined by the built-in junction voltage and the oxide capacitance
  - $V_{GS} > 0$: Ψ_s almost linearly increases with V_{GS}, source starts injecting electrons in the p-region
  - These electrons start to form an n-type channel under the gate and we speak of *weak inversion*
  - These electrons reach the accelerating electrical field of the drain depletion layer due to diffusion and are collected at the drain terminal
  - The $I_{DS}(V_{GS})$ characteristic shows an exponential relationship similar as the $I_C(V_{BE})$ relationship of a lateral bipolar NPN transistor

MOS transistors

Operation, strong inversion

- Brief description of $I_{DS}\left(V_{GS}\right)$ in strong inversion
  - When $V_{GS} > V_T$ the channel extends further under the gate and the Ψ_s does not longer increase significantly with V_{GS}
  - I_{DS} now increases quadratically with $V_{GS} - V_T$
  - The device now operates in *strong inversion*
  - The *threshold voltage* V_T is the gate-source voltage at the transition from weak inversion to strong inversion

MOS transistors

Operation, saturation region and linear region

- If the *effective gate-source* voltage $V_{GS} - V_T$ is below V_{DS} the channel does not extend to the drain.
- In this *pinch-off* or *saturation* region the drain-source current shows a minor dependence on V_{DS} due to the *channel length modulation*
- If V_{GS} increases to V_T above V_{DS} (this is equivalent to: $V_{GD} > V_T$) the channel extends from the source to the drain:
  - I_{DS} becomes strongly dependent on V_{DS}
  - The transistor acts as a controlled resistor and we speak of the *linear operating* region

MOS transistors

Operation, small-geometry effects

With shrinking dimensions in CMOS IC processes, small geometry effects have to be taken into account:

1. The influence of the vertical component of the electrical field in the channel on the charge carrier mobility cannot longer be ignored: VFMR
2. At high lateral field strengths the velocity of the charge carriers saturates.
3. The electrical field in the gate increases with shrinking oxide thickness. This causes a slow change of charge storage in the oxide over time and results in a slow change of V_T over time which may limit the operational life time of CMOS ICs
4. The drain depletion region reaches far and deep under the channel and reduces the channel to bulk depletion capacitance under the channel. This causes a better coupling between V_{GS} and Ψ_s. This *Drain Induced Barrier Lowering* (DIBL) effect causes V_T to decrease with V_{DS} and I_{DS} to increases with V_{DS}

MOSFET modeling

Introduction, first generation models

1. Level 1 model is usually referred to the model presented by Shichman and Hodges:
   - relatively simple first generation MOS model for thick oxide long and wide channel MOSFETs operating in strong inversion
2. Level 2 model is also a first generation model.
   - based on the Level 1 with corrections that account for small geometry effects
3. Level 3 model
   - based on Level 1 model, added equations for small geometry effects have a more empirical character and are more simple than those of the Level 2 model. Also includes basic modeling of weak inversion operation

MOSFET modeling

Introduction, second generation models

1. BSIM (Berkeley Short-Channel IGFET Model) is a second generation MOSFET model
   - focus on fast and robust simulation rather than on a physical basis
2. HSPICE Level 28 model is a second generation model based on the BSIM model. Its improvements strongly facilitated analog CMOS circuit design. It is a proprietary model developed by Meta-Software.
3. BSIM2 model is also a second generation MOSFET model.
   - Improvement of the BSIM model developed by the university of Berkeley.

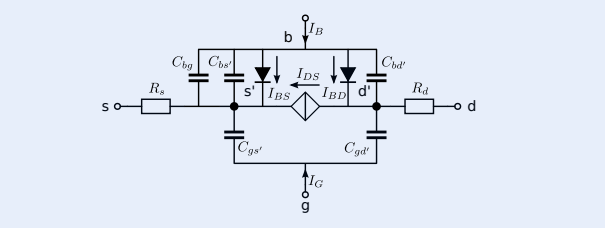
MOSFET modeling

Introduction, third generation models

1. Third generation BSIM3 model includes the geometry parameters in the intrinsic model.
2. MOS Model 9 developed at Philips Laboratories has been made generally available still distinguishes an intrinsic and extrinsic structure, but has improved mathematical modeling.
3. EKV Model has a physical base and takes the bulk node as reference. Source and drain are treated equally yielding a symmetrical model with smooth analytical equations for all operating regions.
4. BSIM4 is suited for analog CMOS design in technology nodes below 100nm.

MOSFET modeling

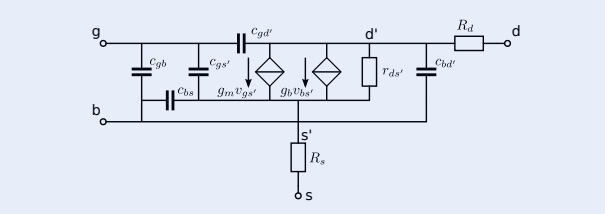
Level 1 model summary



1. Normal mode ($V_{ds} > 0$), cut-off region: $V_{gs} < \mathrm{VTO}$: $I_{ds} = 0$
2. Normal mode ($V_{ds} > 0$), linear region: $V_{gd} > \mathrm{VTO}$: $I_{ds} = \frac{\mathrm{W}}{\mathrm{L}} \mathrm{KP}\, V_{ds} \left(V_{gs} - \mathrm{VTO}\right) \left(1 + \mathrm{LAMBDA}.V_{ds}\right)$
3. Normal mode ($V_{ds} > 0$), saturation region: $V_{gd} < \mathrm{VTO}$: $I_{ds} = \frac{\mathrm{W}}{\mathrm{L}} \frac{\mathrm{KP}}{2} \left(V_{gs} - \mathrm{VTO}\right)^2 \left(1 + \mathrm{LAMBDA}.V_{ds}\right)$

MOSFET modeling

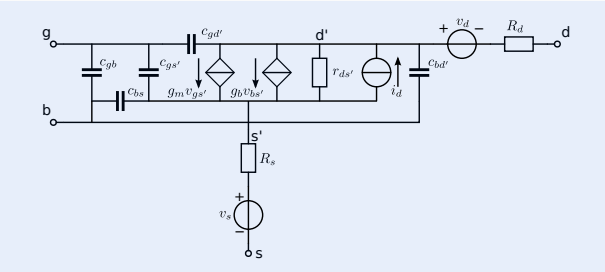
Level 1 small-signal model



- Intrinsic MOS transistor with:
  - g_m and g_b
  - $C_{gs} = \frac{2}{3} C_{ox}$, $C_{gd} = 0$ in saturation region and $C_{gs}, C_{gd} = \frac{1}{2} C_{ox}$ in linear region.
- Junction capacitances
- Bulk resistors

MOSFET modeling

Level 1 small-signal noise model



- Small-signal model with added noise sources:
  - Gate shot noise i_g and channel thermal noise i_{ds}
  - Noise associated with bulk resistors

MOSFET modeling

Level 1 small-signal noise model

Spectral densities S_{vs} and S_{vd}: voltage noise of the bulk resistors R_s and R_d:

$$S_{vs} = 4kTR_s$$
$$S_{vd} = 4kTR_d$$

Noise related to the channel current I_{dsQ}:

$$S_{id} = 4kTg_m\frac{2}{3} + \frac{\mathrm{KF}}{f}I_{dsQ}^{\mathrm{AF}}$$
$$S_{id} = 4kTg_m\frac{2}{3}\left(1 + \frac{f_\ell}{f}\right)$$
$$f_\ell = \frac{3\mathrm{KF}}{8kTg_m}I_{dsQ}^{\mathrm{AF}}$$

f_ℓ Is the corner frequency for the $\frac{1}{f}$ noise.

MOSFET modeling

Level 1 small-signal model parameters

par.	cut-off.	linear region	saturation region
C_{gs}	cgso.w+cgbo.l+ $+\frac{\mathrm{W.L}}{\mathrm{TOX}}\epsilon_{ox}$(max. value)	cgso.w+cgbo.l+ $+\frac{1}{2}\frac{\mathrm{W.L}}{\mathrm{TOX}}\epsilon_{ox}$(max. value)	cgso.w+cgbo.l+ $+\frac{2}{3}\frac{\mathrm{W.L}}{\mathrm{TOX}}\epsilon_{ox}$(max. value)
C_{gd}	cgdo.w	cgdo.w+ $+\frac{1}{2}\frac{\mathrm{W.L}}{\mathrm{TOX}}\epsilon_{ox}$(max. value)	cgdo.w
C_{ds}	cj.ad+cjsw.pd or cbd	cj.ad+cjsw.pd or cbd	cj.ad+cjsw.pd or cbd
g_m	0	$\frac{\mathrm{W}}{\mathrm{L}}.\mathrm{kp}V_{DS}$	$\frac{\mathrm{W}}{\mathrm{L}}.\mathrm{kp}(V_{DS}-\mathrm{VTO}) =$ $=\sqrt{2\frac{\mathrm{W}}{\mathrm{L}}.\mathrm{KP}I_{DS}}$
r_{ds}	∞	$\left[\frac{\mathrm{W}}{\mathrm{L}}.\mathrm{KP}\left(V_{GS}-\mathrm{VTO}\right)\right]^{-1}$ voltage controlled resistor approximation ($V_{DS}=0$)	$1/(\mathrm{lambda}\ I_{DS})$ (lambda $\ll 1$)

MOSFET capacitance modeling

Meyer Model

Linear region:

$$c_{gs'} = \frac{2}{3}\mathrm{W.L}C_{ox}\left(1 - \frac{(V_{gd'} - V_t)^2}{(V_{gs'} - V_t + V_{gd'} - V_t)^2}\right) + \mathrm{CGSO.W}$$

$$c_{gd'} = \frac{2}{3}\mathrm{W.L}C_{ox}\left(1 - \frac{(V_{gs'} - V_t)^2}{(V_{gs'} - V_t + V_{gd'} - V_t)^2}\right) + \mathrm{CGDO.W}$$

$$c_{gb} = 0$$

Saturation region:

$$c_{gs'} = \frac{2}{3}\mathrm{W.L}C_{ox} + \mathrm{CGSO.W},\ c_{gd'} = \mathrm{CGDO.W},\ c_{gb} = 0$$

Cut-off region we have:

$$c_{gs'} = \mathrm{CGSO.W},\ c_{gd'} = \mathrm{CGDO.W},\ c_{gb} = \mathrm{W.L}C_{ox} + \mathrm{CGBO.L}\ (\text{max. } V_{GB} = 0)$$

MOSFET capacitance modeling

Ward-Dutton capacitance model

- Ward and Dutton use a capacitance matrix that relates the four dynamic terminal currents of the intrinsic transistor to the terminal voltages:

$$\begin{pmatrix} i_g \\ i_d \\ i_s \\ i_b \end{pmatrix} = s \begin{pmatrix} C_{GG} & -C_{GD} & -C_{GS} & -C_{GB} \\ -C_{DG} & C_{DD} & -C_{DS} & -C_{DB} \\ -C_{SG} & -C_{SD} & C_{SS} & -C_{SB} \\ -C_{BG} & -C_{BD} & -C_{BS} & C_{BB} \end{pmatrix} \begin{pmatrix} v_g \\ v_d \\ v_s \\ v_b \end{pmatrix}$$

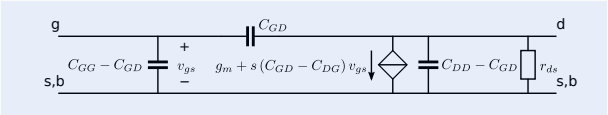
where i_g, i_d, i_s and i_b are the terminal currents of the intrinsic transistor and v_g, v_d, v_s and v_b the corresponding intrinsic terminal voltages.

MOSFET capacitance modeling

Ward-Dutton capacitance model and hybrid-pi model

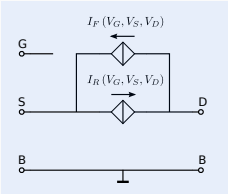
- If source and bulk are connected together and taken as reference, we have $v_s = 0$ and $v_b = 0$ and the matrix simplifies to:

$$\begin{pmatrix} i_g \\ i_d \end{pmatrix} = s \begin{pmatrix} C_{GG} & -C_{GD} \\ (C_{GD} - C_{DG}) - C_{GD} & C_{DD} \end{pmatrix} \begin{pmatrix} v_{gs} \\ v_{ds} \end{pmatrix}$$



MOSFET modeling

EKV model summary



- Model developed by Ernst and Vittoz
- Physical basis
- Voltage-controlled expression for the channel current $I_{DS}(V_{SB}, V_{GB}, V_{DB})$ for all regions of operation
- Application of Inversion Coefficient for design described by Binkley

MOSFET modeling

EKV model: technology current

Binkley defines the technology current I_0 as:

$$I_0 = 2n\mu_0 C'_{OX} U_T^2 \text{ [A]}$$

substrate factor n:

$$n \approx 1 + \frac{C'_{DEP}}{C'_{OX}} \text{ [-]}$$

oxide capacitance per unit of area C'_{OX}:

$$C'_{OX} = \frac{\varepsilon_o \varepsilon_r}{t_{ox}} \text{ [Fm}^{-2}\text{]}$$

ε_r is the relative permittivity of SiO_2, t_{ox} is the thickness of the gate oxide and U_T is the thermal voltage. C'_{DEP} is the surface depletion capacitance.

MOSFET modeling

EKV model: transconductance factor

The transconductance factor β_{sq} is defined as:

$$\beta_{sq} = \mu_0 C'_{OX} \text{ [AV}^{-2}\text{m}^{-2}\text{]}$$

μ_0 is the low-field channel carrier mobility in $[\text{m}^2\text{V}^{-1}\text{s}^{-1}]$.
The technology current can be expresses in β_{sq} as:

$$I_0 = 2n\beta_{sq}U_T^2 \text{ [A]}$$

MOSFET modeling

EKV model: weak inversion

In weak inversion the forward drain-source current I_F shows an exponential relation with the gate voltage:

$$I_{F,R} = I_0 \exp\left(\frac{\frac{V_G - V_{T0}}{n} - V_{S,D}}{U_T}\right) \text{ [A]}$$

The voltage V_{T0} is the *equilibrium threshold voltage*. The pinch-off voltage V_P is defined as:

$$V_P = \frac{V_G - V_{T0}}{n} \text{ [V]}$$

MOSFET modeling

EKV model: strong inversion

In strong inversion the currents depend quadratically on the driving voltage:

$$I_{F,R} = \frac{W}{L}\frac{\beta_{sq}}{2n}\left(V_G - V_{T0} - nV_{S,D}\right)^2 \text{ [A]}$$

Where W and L are the effective width and length of the channel, respectively.

MOSFET modeling

EKV model: weak inversion to strong inversion

With the aid of a transition function $F(x)$, the expressions for weak inversion and strong inversion can be combined into one:

$$F(x) = \left(\ln\left(1+\exp\left(\frac{x}{2}\right)\right)\right)^2 \text{ [-]}$$
$$= \begin{array}{ll} \exp(x) & \text{if } x \ll 0 \\ \left(\frac{x}{2}\right)^2 & \text{if } x \gg 0 \end{array}$$

This function returns the forward and the reverse *inversion coefficients*, IC_F and IC_F:

$$IC_{F,R} = F\left(\frac{V_G - V_{T0} - nV_{S,D}}{nU_T}\right) \text{ [-]}$$

MOSFET modeling

EKV model: inversion coefficients

- The inversion coefficients are a measure for the level of inversion at which the transistor operates.
- An inversion coefficient much smaller than unity indicates weak inversion.
- An inversion coefficient much larger than unity indicates operation in strong inversion.
- Between weak and strong inversion we speak of moderate inversion.
- The actual forward and reverse current can be calculated from their respective inversion coefficients as:

$$I_{F,R} = I_0 \frac{W}{L} IC_{F,R} \text{ [A]}$$

- Or, alternatively:

$$I_{F,R} = 2n\beta_{sq} U_T^2 \frac{W}{L} IC_{F,R} \text{ [A]}$$

MOSFET modeling

EKV model: VFMR

- VFMR is modeled as reduction of the transconductance factor β_{sq} due to the gate-source voltage.
- A simple mobility reduction model uses the vertical field mobility reduction factor θ [V^{-1}].

$$\beta'_{sq} = \frac{\beta_{sq}}{1 + \theta V_P} \ [AV^{-2}m^{-2}]$$

- With this expression β'_{sq} increases below threshold and has a singularity at $\theta V_P = -1$.
- This can be corrected by softly clipping the VFMR effect below threshold:

$$\beta'_{sq} = \frac{\beta_{sq}}{1 + 2\theta U_T \sqrt{IC_F}} \ [AV^{-2}m^{-2}]$$

MOSFET modeling

EKV model: CLM

- The channel length modulation can be modeled with an Early voltage. The Early voltage V_A is approximately proportional with the length of the device:

$$V_A = V_{AL} L \text{ [-]}$$

  Where V_{AL} [Vm^{-1}] is the Early voltage per unit of length.

- After including the CLM the expression of the drain-source current I_{DS} changes to:

$$I_{DS} = (I_F - I_R)\left(1 + \frac{V_S - V_D}{V_{AL} L}\right) \text{ [A]}$$

  For reverse operation V_S and V_D should be swapped.

MOSFET modeling

EKV model: Velocity Saturation

- Binkley describes the modeling of velocity saturation for the saturation region through introduction of a second term in β_{sq}:

$$\beta'_{sq} = \frac{\beta_{sq}}{1 + \left(\theta + \frac{1}{E_{CRIT} L}\right) 2 U_T \sqrt{IC_F}} \ [\mathrm{AV^{-2}m^{-2}}]$$

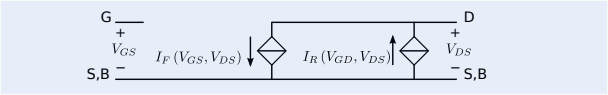
  Where E_{CRIT} [$\mathrm{Vm^{-1}}$] is the value of the lateral field at which velocity saturation occurs.

- At a later stage we will use the critical inversion coefficient IC_{CRIT}: the inversion coefficient at which the reduction of the mobility due to VFMR and velocity sets in:

$$IC_{CRIT} \approx \frac{1}{\left(4 n U_T \left(\theta + \frac{1}{L \ E_C}\right)\right)^2} \ [-]$$

MOSFET modeling

EKV model: Static device characteristics



- In the saturation region I_R can be ignored. If we discard velocity saturation and CLM and take $V_S = 0$ we obtain the Level 1 model equation for the saturation region:

$$I_{DS} = \frac{W}{L}\frac{\beta_{sq}}{2n}\left(V_{GS} - V_{T0}\right)^2 \text{ [A]}$$

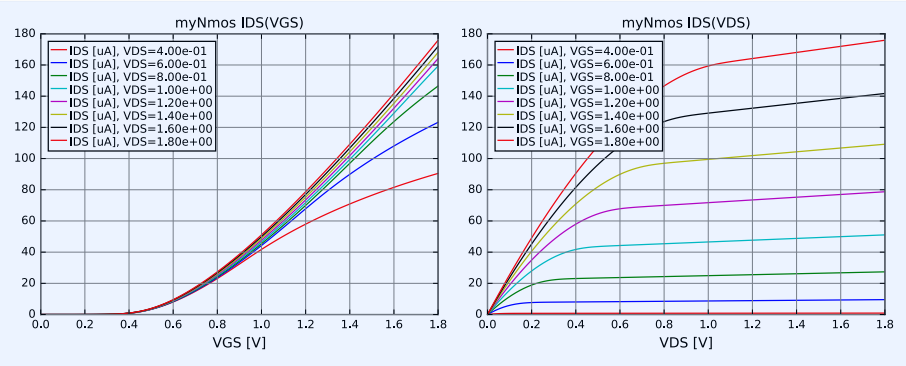
- In the linear region we cannot ignore the reverse current component. With $V_S = 0$ we obtain the Level 1 model equation for the linear region:

$$I_{DS} = \frac{W}{L}\frac{\beta_{sq}}{n}V_D\left(V_{GS} - V_{T0} - \frac{1}{2}V_{DS}\right) \text{ [A]}$$

MOSFET modeling

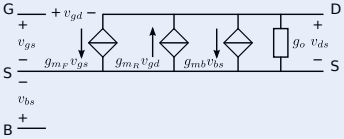
EKV model: Static device characteristics

NMOS transistor `myNMOS` ($W = 220$nm, $L = 180$nm) calculated according to the above (simplified) model with parameters of a standard CMOS18 process as listed by Binkley.



MOSFET modeling

EKV model: Small-signal model transconductance

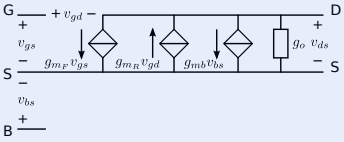


- Binkley saturation region:

$$g_{m_F} = \frac{I_F \left(1 + \frac{V_S - V_D}{V_{AL} L}\right)}{nU_T \sqrt{IC_F \left(1 + \frac{IC_F}{IC_{CRIT}}\right)} + 0.5 \sqrt{IC_F \left(1 + \frac{IC_F}{IC_{CRIT}}\right)} + 1} \ [\mathrm{AV}^{-1}]$$

MOSFET modeling

EKV model: Small-signal model transconductance



- Reverse transconductance approximation (incorrect modeling of velocity saturation)

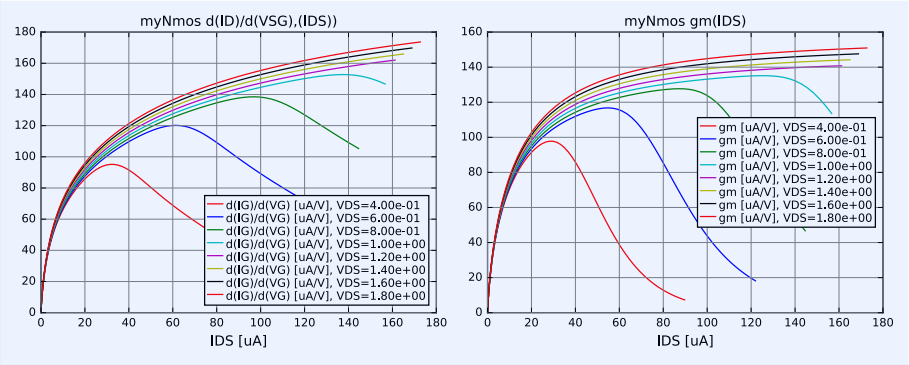
$$g_{m_R} = \frac{I_R}{nU_T\sqrt{IC_R\left(1+\frac{IC_R}{IC_{CRIT}}\right)}+0.5\sqrt{IC_R\left(1+\frac{IC_R}{IC_{CRIT}}\right)}+1} \ [AV^{-1}]$$

- The total transconductance is found as the difference between the two:

$$g_m = g_{m_F} - g_{m_R} \ [\mathrm{AV}^{-1}]$$

MOSFET modeling

EKV model: Small-signal model transconductance

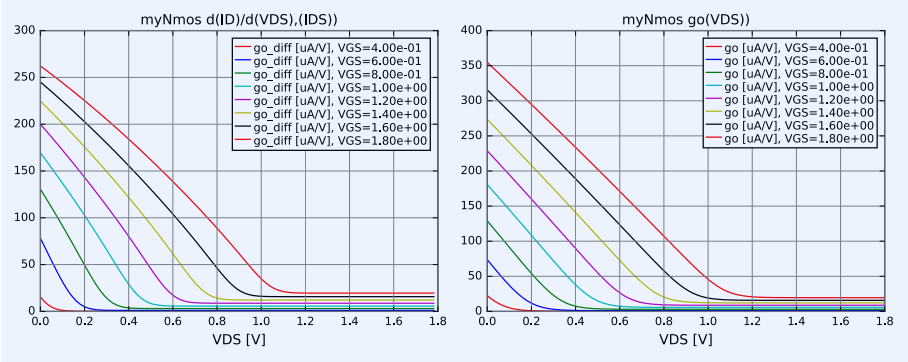


MOSFET modeling

EKV model: Output conductance

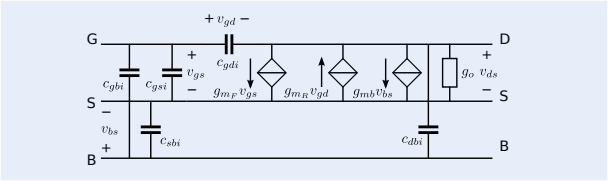
- Approximation (no DIBL)

$$g_{ds} = \frac{V_{DS} + V_{AL}L}{I_{DS}} + \frac{\beta_{sq} U_T}{1 + 2\theta U_T \sqrt{IC_F}} \frac{W}{L} 2\sqrt{IC_R} \qquad (1)$$



MOSFET modeling

EKV model: Small-signal intrinsic capacitances



The intrinsic capacitances can be expressed as a part of the total oxide capacitance C_{OX}:

$$C_{OX} = WLC'_{OX} \text{ [F]}$$

The SPICE EKV2.6 model uses two parameters for calculation of these relative parts:

$$x_f = \sqrt{\frac{1}{4} + IC_F} \text{ [-]} \ , \ x_r = \sqrt{\frac{1}{4} + IC_R} \text{ [-]}$$

MOSFET modeling

EKV model: Small-signal intrinsic capacitances

The intrinsic capacitances are:

$$c_{gsi} = \frac{2}{3}\left(1 - \frac{x_r^2 + x_r + \frac{1}{2}x_f}{(x_r + x_f)^2}\right) C_{OX} \text{ [F]}$$

$$c_{gdi} = \frac{2}{3}\left(1 - \frac{x_f^2 + x_f + \frac{1}{2}x_r}{(x_r + x_f)^2}\right) C_{OX} \text{ [F]}$$

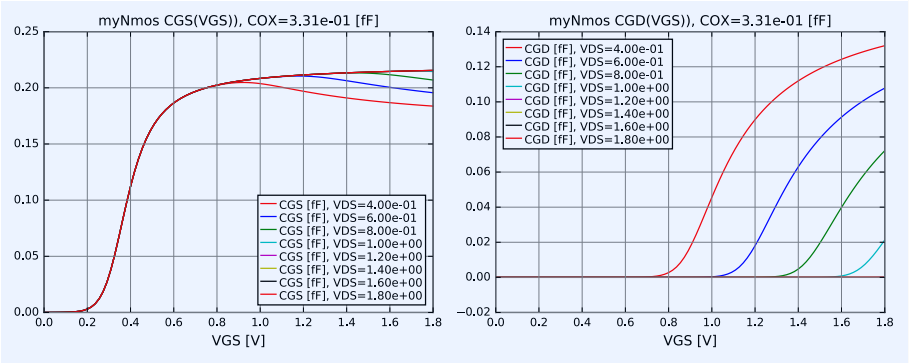
$$c_{gbi} = \frac{n-1}{n}\left(C_{OX} - c_{gsi} - c_{gdi}\right) \text{ [F]}$$

$$c_{sbi} = (n-1)\, c_{gsi} \text{ [F]}$$

$$c_{sdi} = (n-1)\, c_{gdi} \text{ [F]}$$

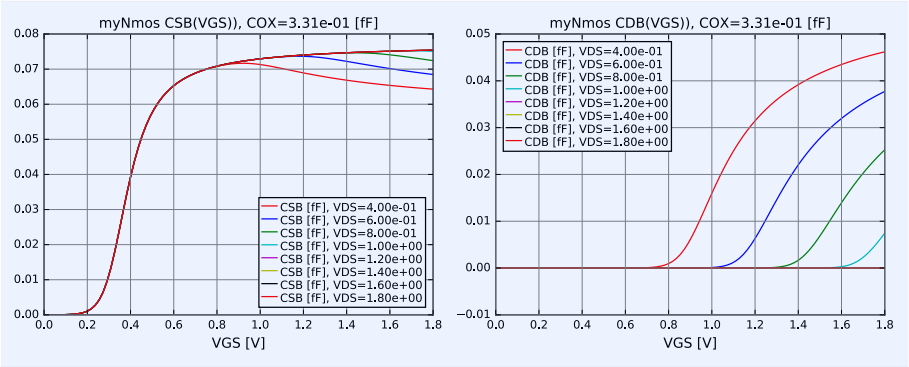
MOSFET modeling

EKV model: Small-signal intrinsic capacitances



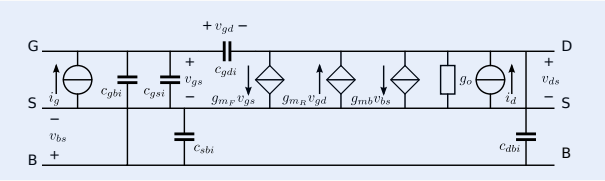
MOSFET modeling

EKV model: Small-signal intrinsic capacitances



MOSFET modeling

EKV model: Intrinsic noise model



MOSFET modeling

EKV model: Intrinsic noise model

- The spectral density S_{i_g} of the shot noise i_g associated with the gate leakage current I_G

$$S_{i_g} = 2qI_G\left(1 + \frac{f_{\ell g}}{f}\right) \ [\mathrm{A^2Hz^{-1}}]$$

- The spectral density of i_d differs for the linear and the saturation region.
- In the linear region ($V_{DS} < V_{DS,sat}$) the spectral density S_{id} is that of a resistor with resistance $\frac{1}{g_o}$:

$$S_{i_{d,lin}} = 4kTg_o \ [\mathrm{A^2Hz^{-1}}]$$

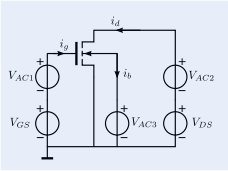
- In the saturation region, the spectral density S_{id} can be written as:

$$S_{id,sat} = 4kTn\Gamma g_m \ [\mathrm{A^2Hz^{-1}}]$$

- Where $\Gamma = \frac{2}{3}$ in strong inversion ...

Determination of small-signal parameters

Simulation test bench



1. Bias the device in the required operating point with V_{GS} and V_{DS}
2. Add an AC signal (`AC 1 0`) to V_{AC1} only
3. Perform an AC analysis over the frequency range of interest
4. Obtain the following small-signal parameters:

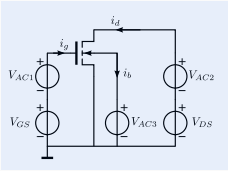
$$g_m = \mathrm{Re}\{I(V_{AC2})\}$$

$$C_{gg} = C_{iss} = -\frac{\mathrm{Im}\{I(V_{AC1})\}}{2\pi f}$$

$$C_{gb} = \frac{\mathrm{Im}\{I(V_{AC3})\}}{2\pi f}$$

Determination of small-signal parameters

Simulation test bench



1. Now add the AC signal (`AC 1 0`) to V_{AC3} only
2. Perform an AC analysis over the frequency range of interest
3. Obtain the following small-signal parameters:

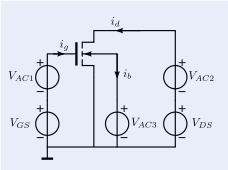
$$g_{mb} = \mathrm{Re}\{I(V_{AC2})\}$$

$$C_{bs} = -\frac{\mathrm{Im}\{I(V_{AC1})\}}{2\pi f}$$

$$C_{bd} = -\frac{\mathrm{Im}\{I(V_{AC2})\}}{2\pi f}$$

Determination of small-signal parameters

Simulation test bench



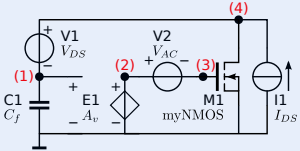
1. Now add the AC signal (`AC 1 0`) to V_{AC2} only
2. Perform an AC analysis over the frequency range of interest
3. Finally obtain the following small-signal parameters:

$$g_o = \frac{1}{r_{ds}} = -\operatorname{Re}\{I(V_{AC2})\}$$

$$C_{dg} = -\frac{\operatorname{Im}\{I(V_{AC1})\}}{2\pi f}$$

Determination of cut-off frequency

Simulation test bench



- PSPICE and SIMETRIX parametric analysis with goal functions:
  - `XatNthY(<expr>, <yValue>, <crossingNR>)`
  - `expr`: $\frac{I_D}{I_G} = \frac{I(V_1)}{I(V_2)}$
  - `yValue`: 1
  - `crossingNR`: 1